

# Drax MLK/Rocket MLK 11.6" Schematic

## Stoney Ridge FT4

2018-01-02

REV : A00

*DY : None Installed*

*OSP/1SP : different config for storage*

Drax Rocket MLK



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Title

**Cover Page**

Size  
A3

Document Number

**Drax MLK/Rocket MLK AMD**

Rev

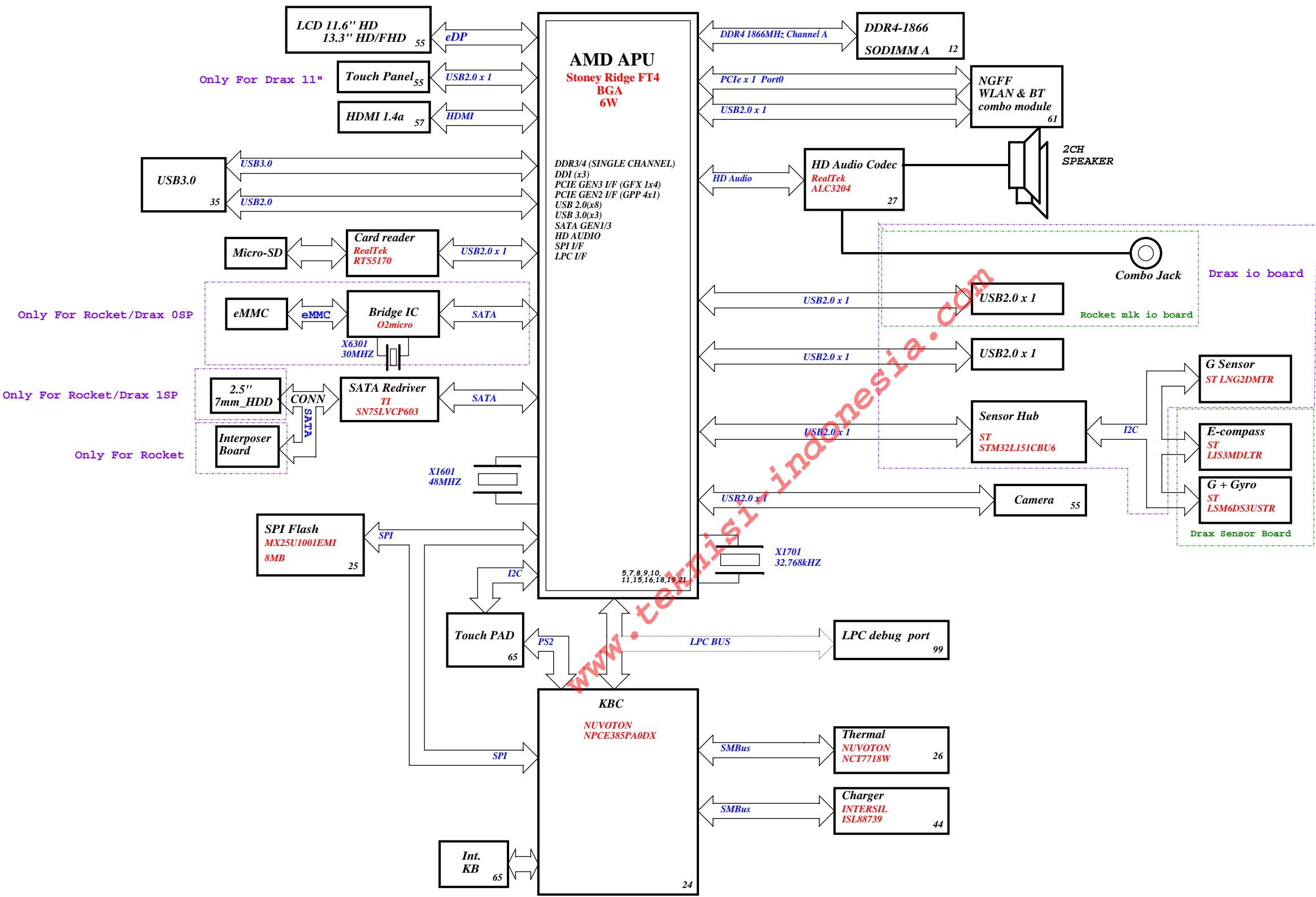
**A00**

Date: Tuesday, January 02, 2018

Sheet 1 of 109

Project code : 4PD0DW010001-->Drax MLK\_17877  
4PD0E2010001-->Rocket MLK\_17876  
PCB P/N : 17837  
Revision : -1

Drax MLK/Rocket MLK\_AMD Stoney Ridge Block Diagram



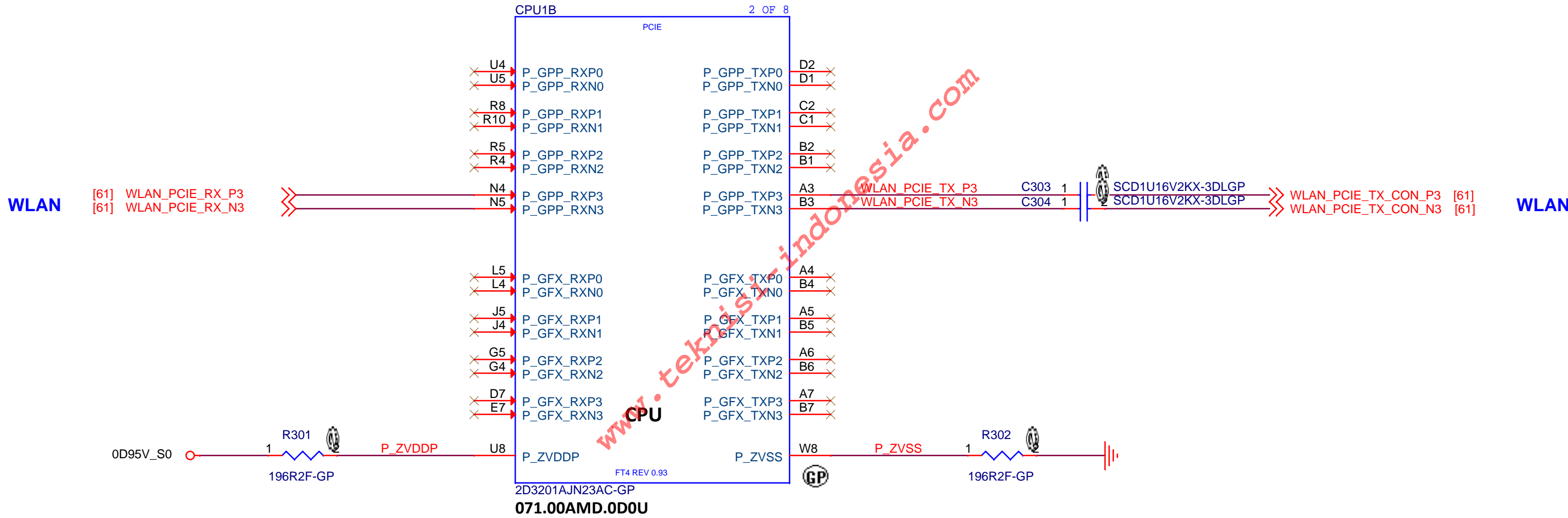
CHARGER		
ISL88739HRZ-T		44
INPUTS	OUTPUTS	
AD+ 12V_BT+	DCBATOUT	
SYSTEM DC/DC		
RT6575DGQW		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5 5V_AUX_S5	
CPU Core Power		
ISL62771HRTZ		46-47
INPUTS	OUTPUTS	
DCBATOUT	1V_CPU_CORE 1D2V_CPU_VDDNB	
DDR4 SUS		
G5388K11U		53
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
CPU VDDP		
G5388K11U		52
INPUTS	OUTPUTS	
DCBATOUT	0D95V_S5	
CPU VDD18		
RT5797ALGQW RT9078-18GJ5		54
INPUTS	OUTPUTS	
3D3V_S5 3D3V_AUX_S5	1D8V_S5 1D8V_AUX_S5	
CPU VDDCRGFX		
APL5337KAI		49
INPUTS	OUTPUTS	
1D8V_S5	0D775V_S5	
Switches		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5 1D8V_S5 0D95V_S5	5V_S0 3D3V_S0 1D8V_S0 0D95V_S0	

PCB LAYER	
L1:Top L2:VCC L3:Signal	L4:Signal L5:GND L6:Bottom


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SSID = CPU

GPP CLK port	Device	CLKREQ#
3	WLAN	3



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SSID = CPU

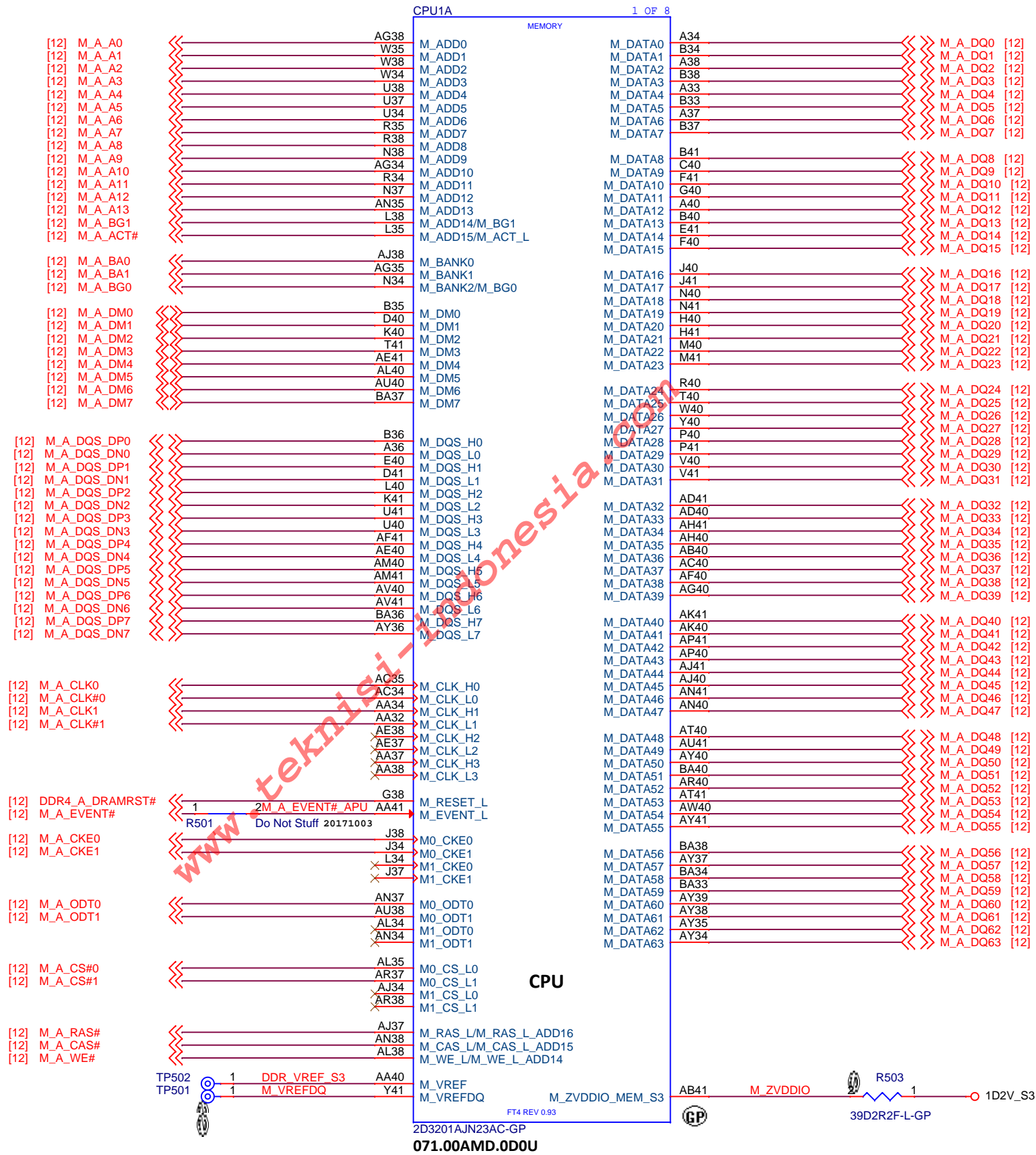
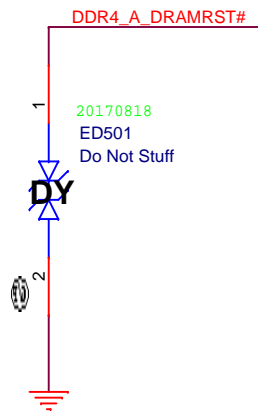
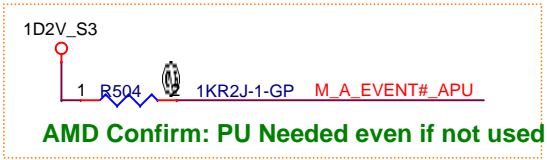
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SSID = CPU



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Title

CPU (DDR)

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SSID = CPU

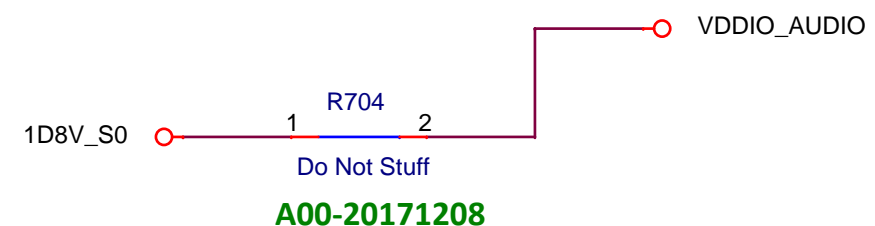
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**SSID = CPU**





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**Rev**  
*A00*

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**Title**

***CPU(VCC\_CORE)***

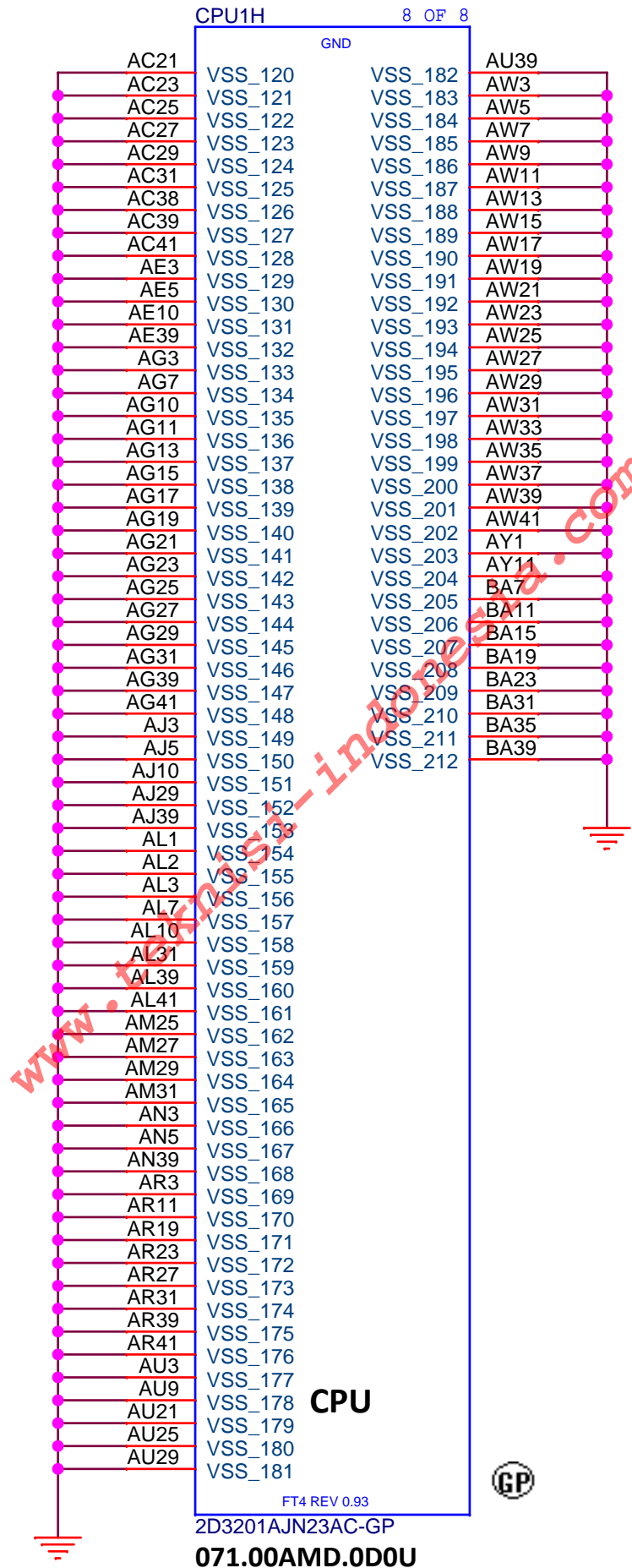
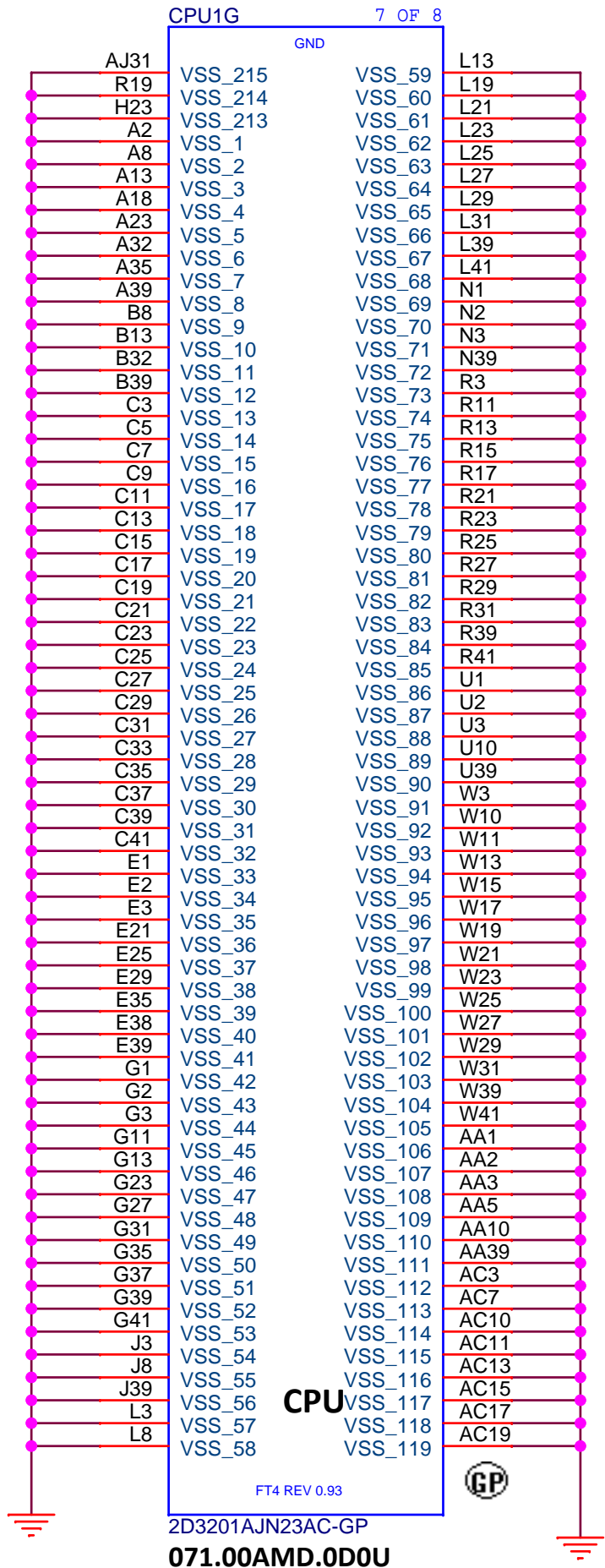
<b>Size</b> A4	<b>Document Number</b> <i><b>Drax MLK/Rocket MLK AMD</b></i>	<b>Rev</b> <i><b>A00</b></i>
<b>Date:</b> Tuesday, January 02, 2018	<b>Sheet</b> 7 <b>of</b>	106







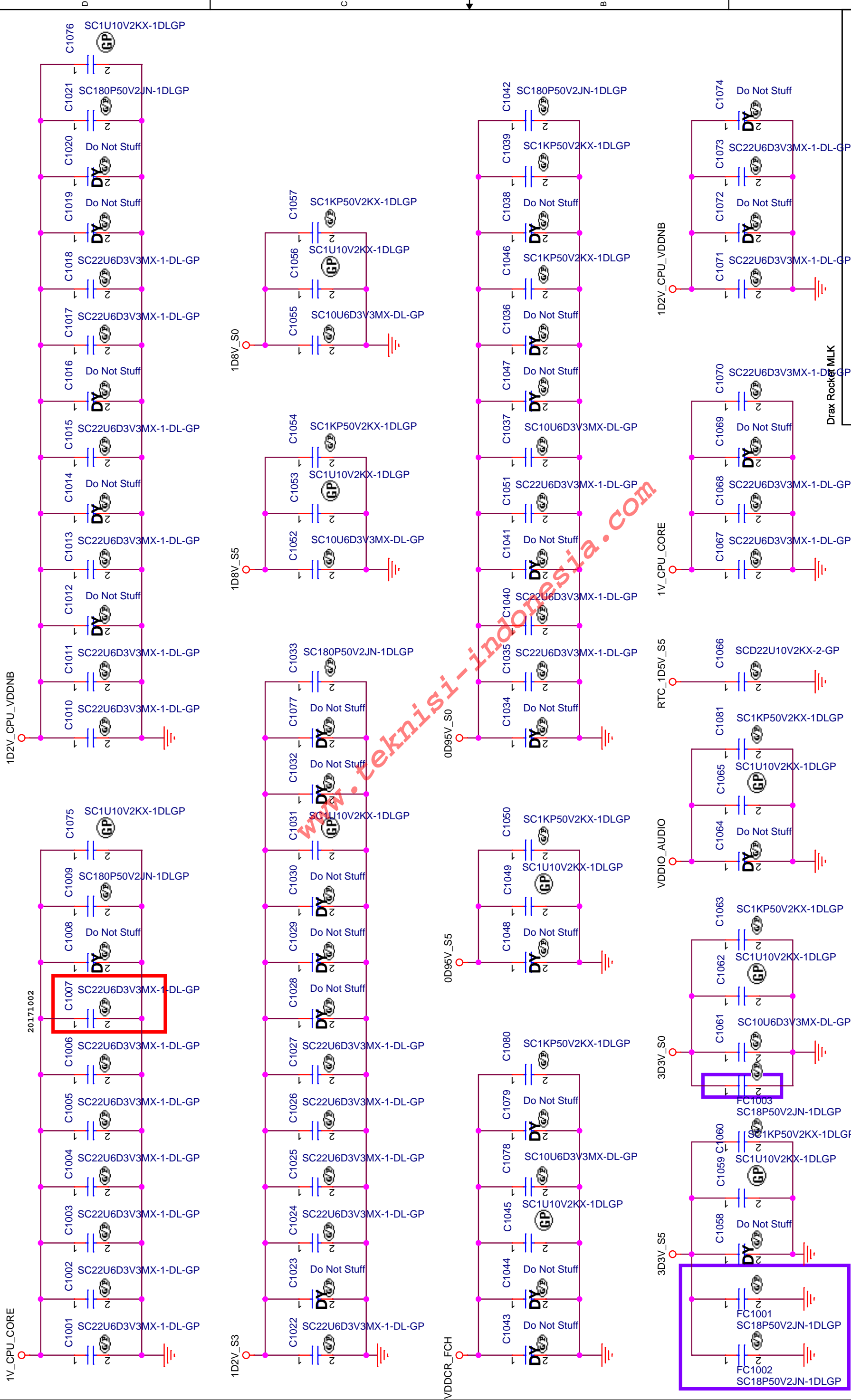
SSID = CPU



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Title <b>CPU (VSS)</b>					
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RF request  
20171103

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Title		Document Number	Rev
CPU (Power CAP1)		Drax MLK/Rocket MLK AMD	A00
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SSID = CPU

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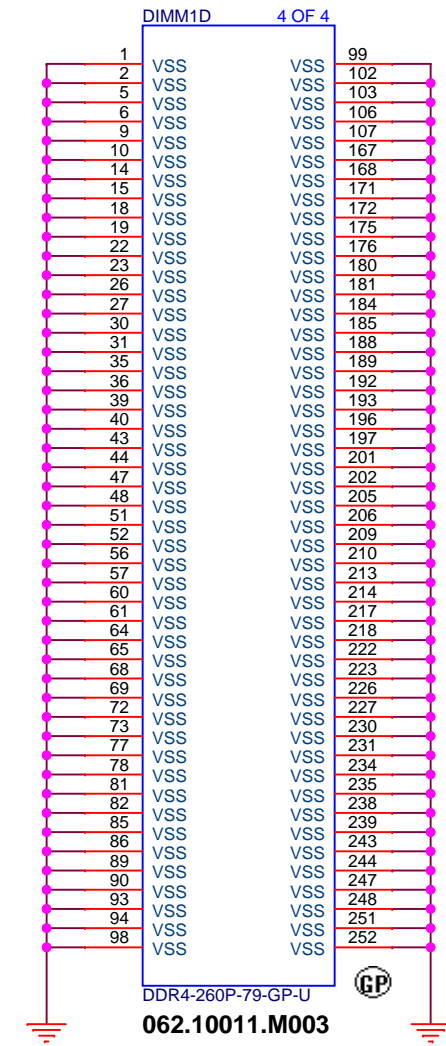
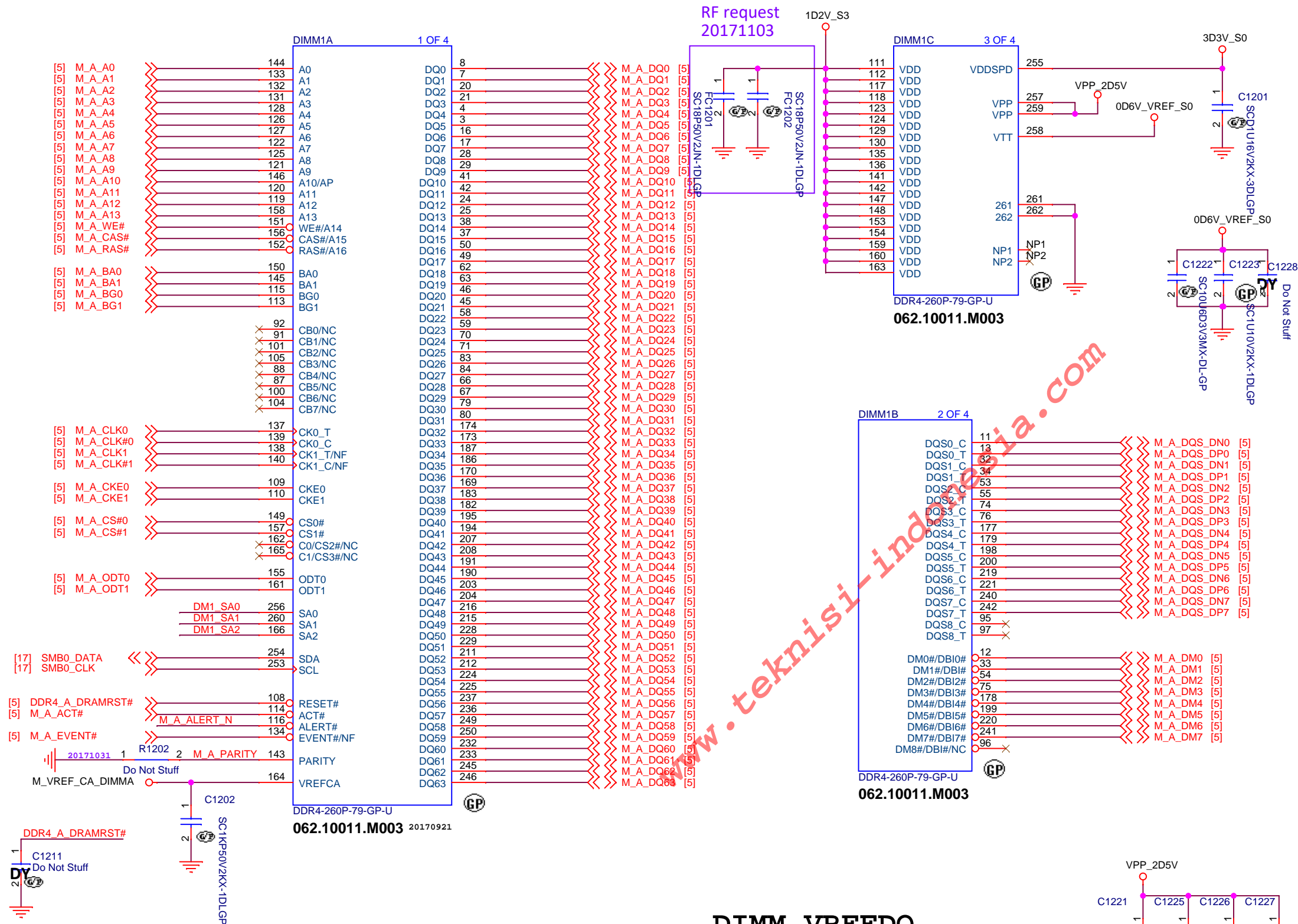
Size  
A4

Document Number  
**Drax MLK/Rocket MLK AMD**

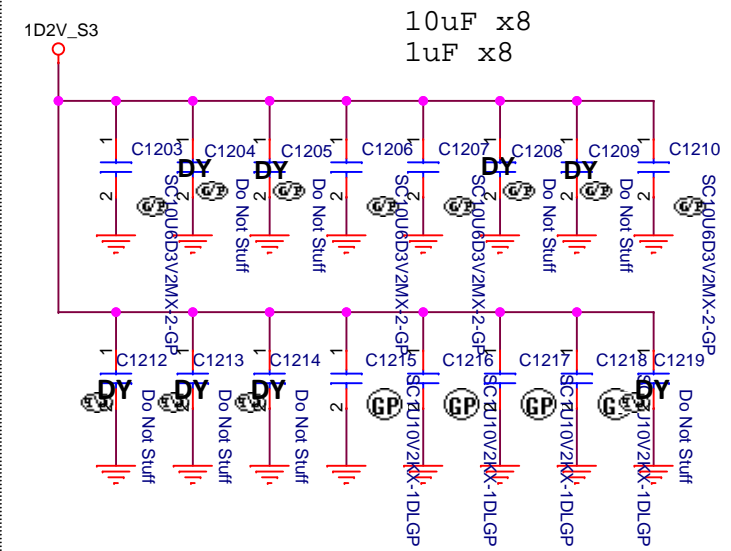
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**A00**

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**SSID = DDR4-SODIMM1**



Layout Note :  
Place these Caps near DIM1



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**DDR4-SODIMM1**

Size

Document Number

A3	<b>Drax MLK/Rocket MLK AMD</b>
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Rev

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Sheets

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106


SPD Address of DIMMA

SPD SA2	0
SPD SA1	0
SPD SA0	0

SSID = DDR4-SODIMM2

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SSID = CPU

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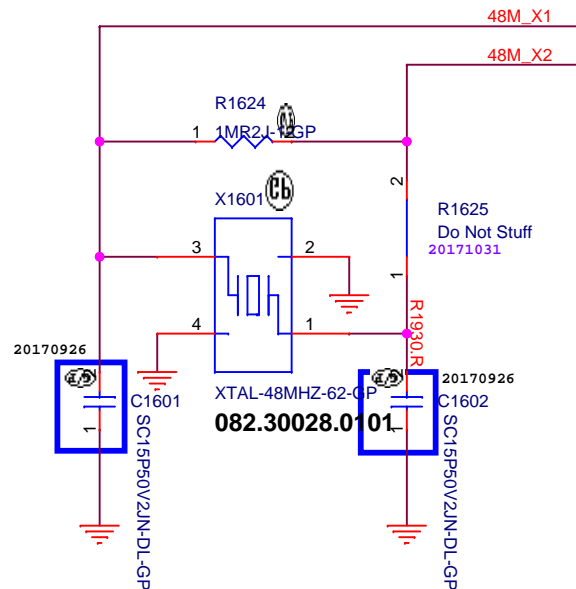
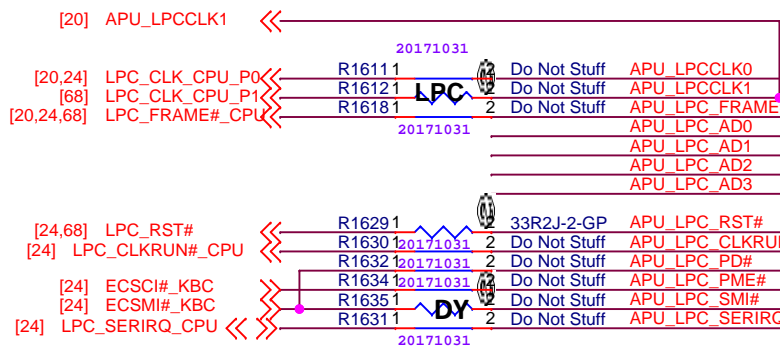
**SSID = CPU**



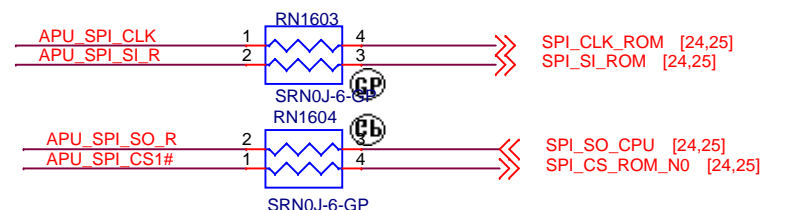
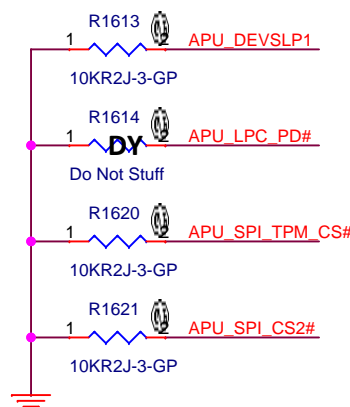
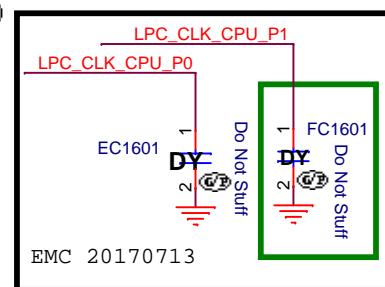
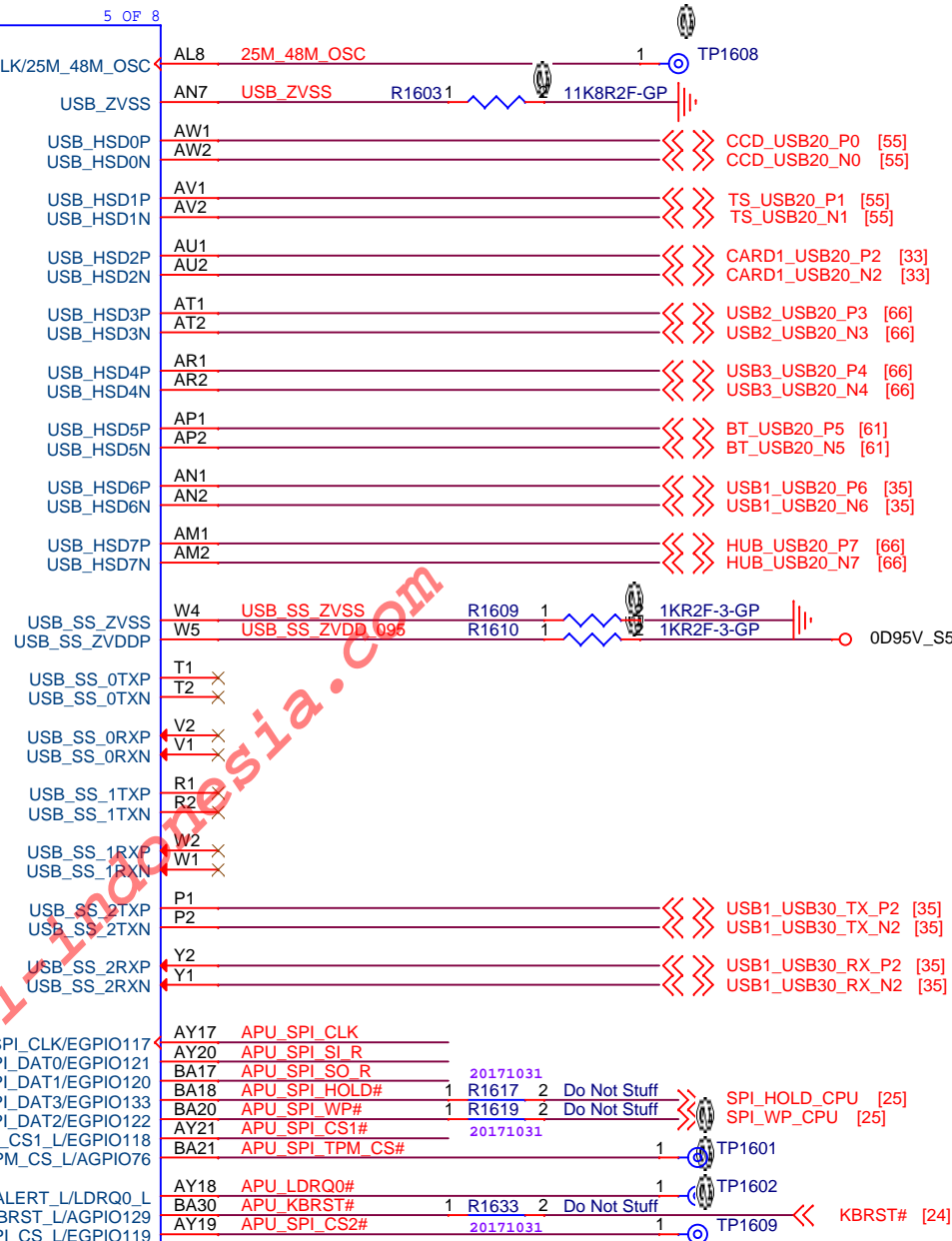
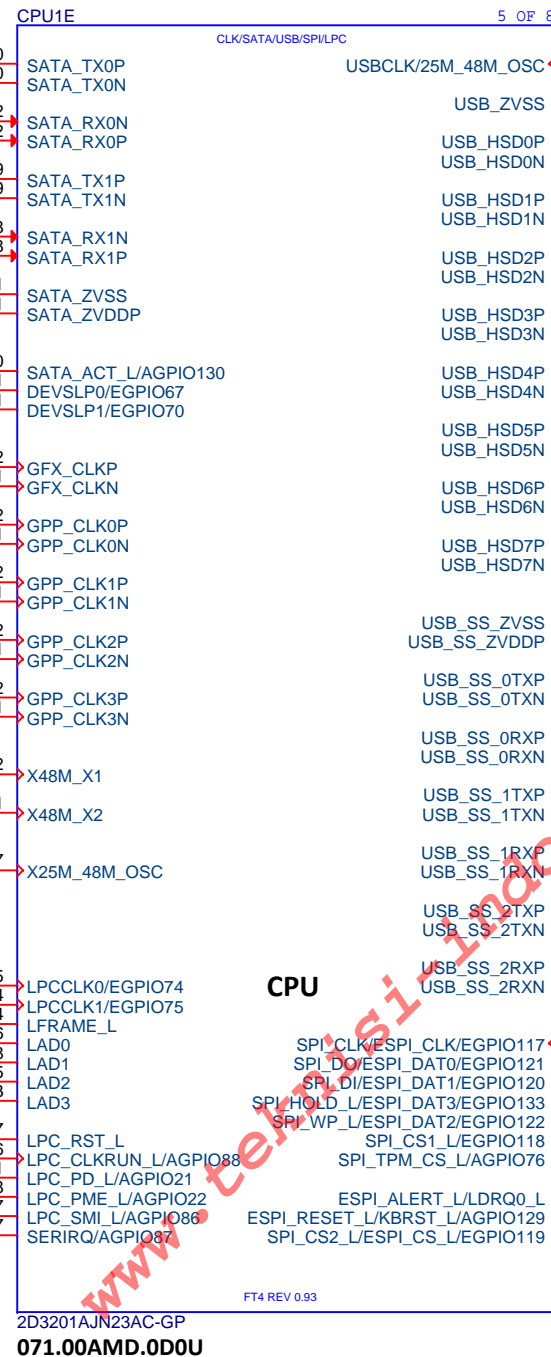
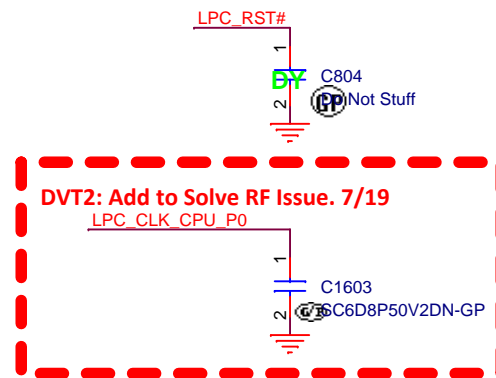
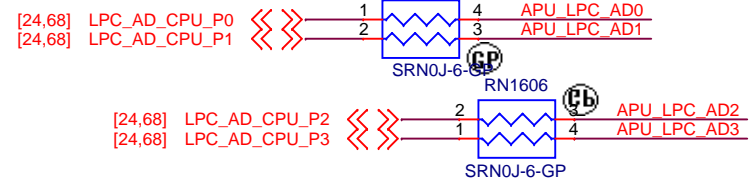
SATA	
Pair	Device
0	HDD/SSD
1	eMMC



GPP CLK port	Device	CLKREQ#
3	WLAN	3



	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M

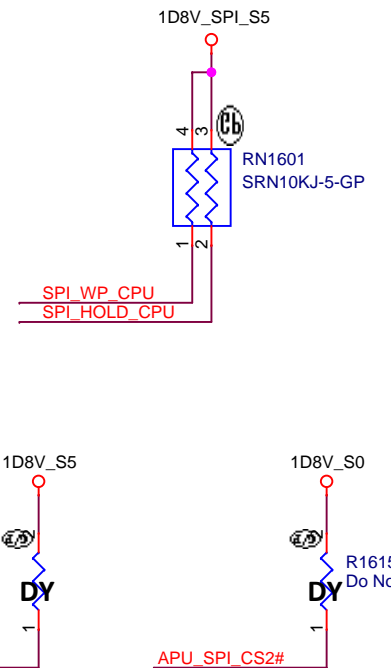


## USB Table

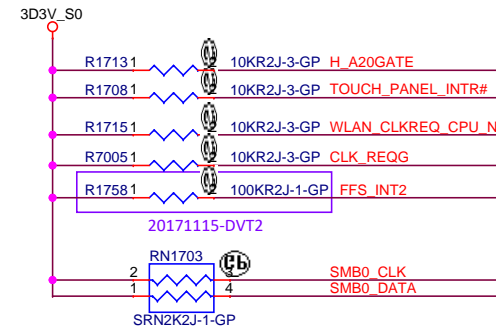
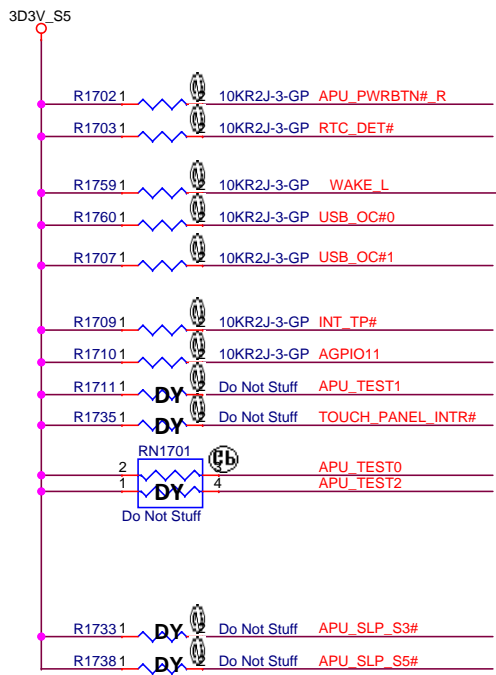
Pair	Device
0	camera
1	Touch Panel (IOBD Conn.)
2	Card Reader
3	USB2.0 (IOBD Conn.)
4	USB2.0 (IOBD Conn.)
5	BT(NGFF)
6	USB3.0(MB port2)
7	Sensor Hub (IOBD Conn.)

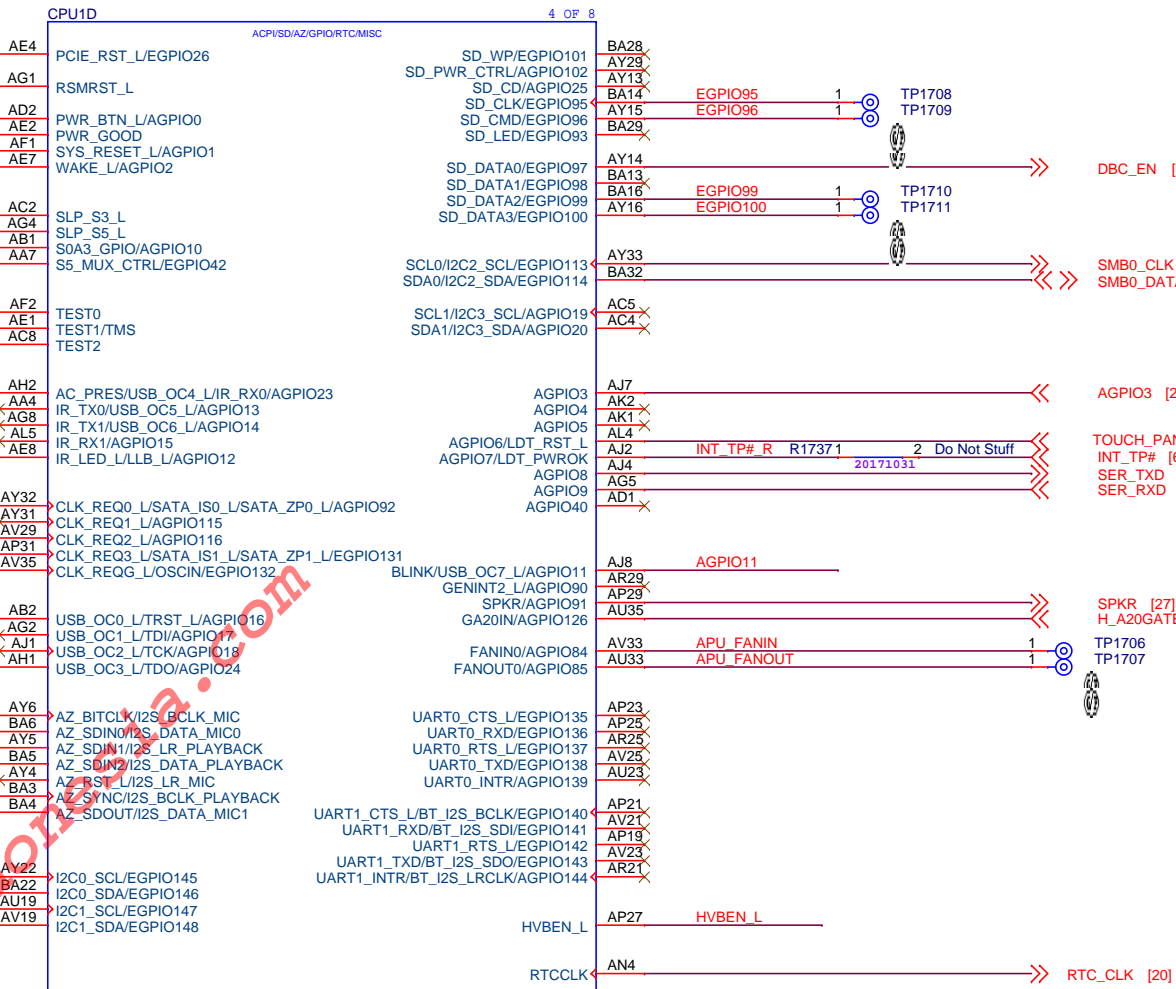
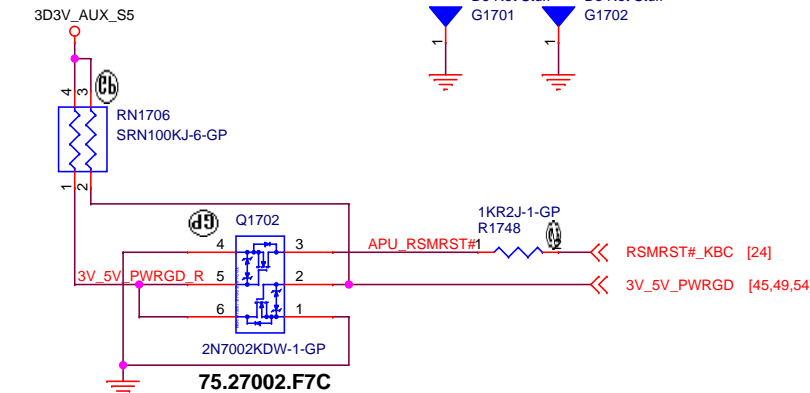
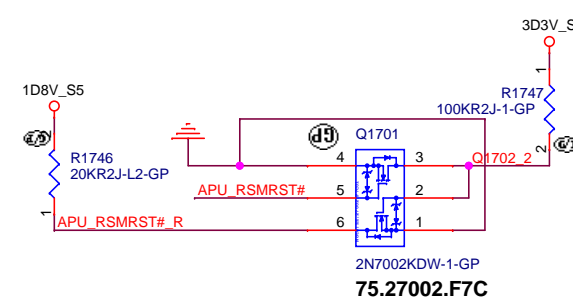
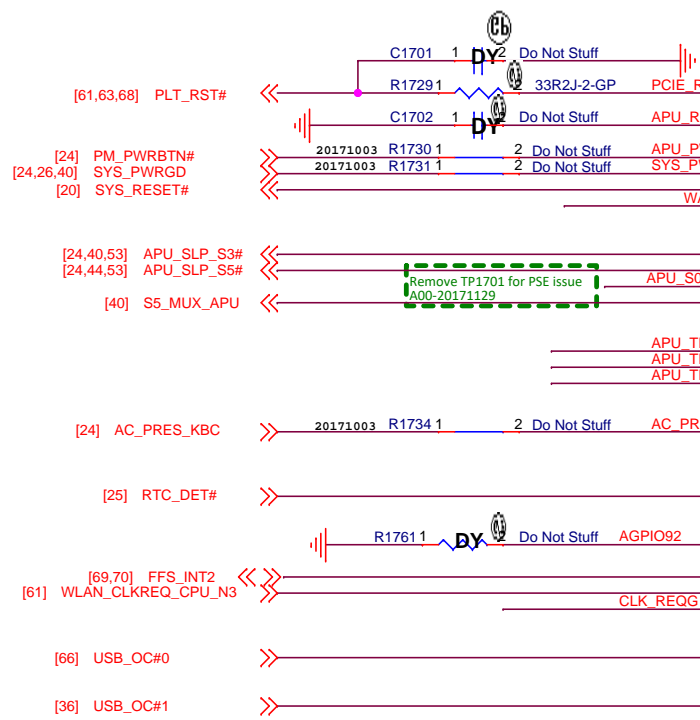
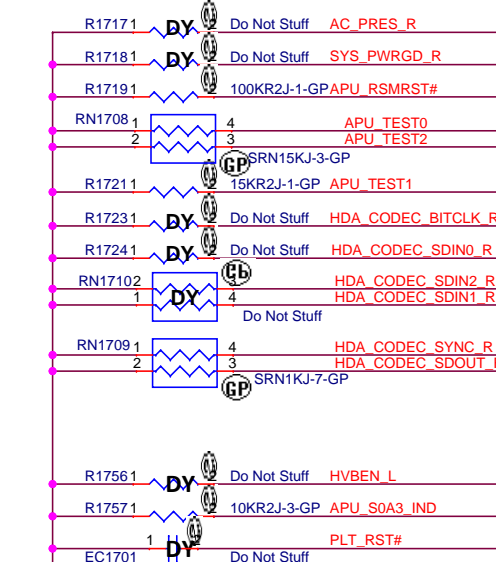
0	NA
1	NA
2	USB3.0(MB port2)



SSID = CPU



Pull-up 10Kohm if not used.



Drax Rocket MLK

**DELL** Wistron Corporation  
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Title **CPU(ACPI/SD/AZ/GPIO/RTC)**

Size Custom Document Number **Drax MLK/Rocket MLK AMD** Rev **A00**

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SSID = CPU

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SSID = CPU

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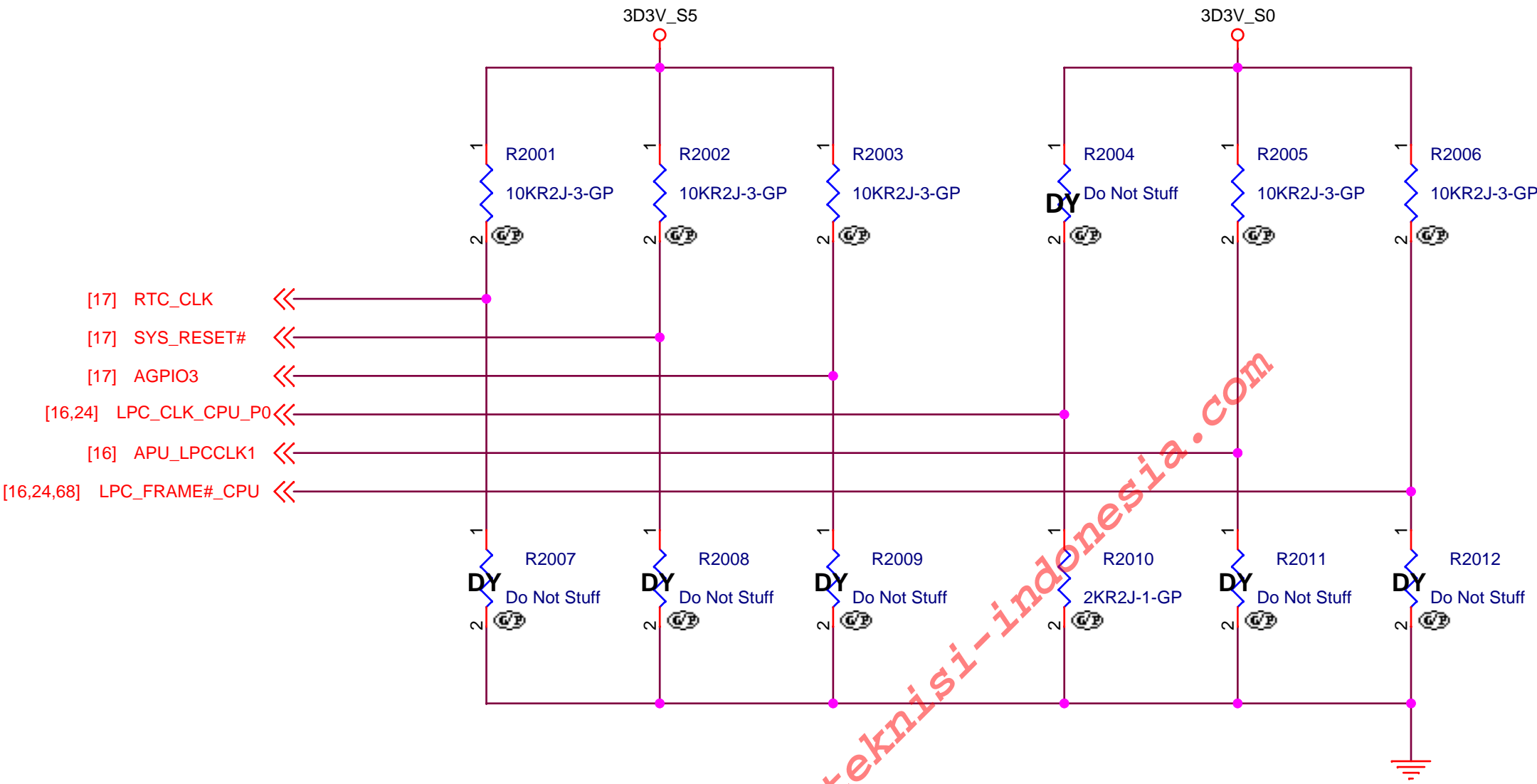
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SSID = STRAPPING

SYSTEM STRAPPINGS



REQUIRED SYSTEM STRAPS

	RTC_CLK	SYS_RESET#	AGPIO3	LPC_CLK0	LPC_CLK1	LPC_FRAME#
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

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Title

**CPU Strappings**

Size  
A4

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Rev  
**A00**

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SSID = CPU

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Rev  
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SSID = CPU

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SSID = CPU

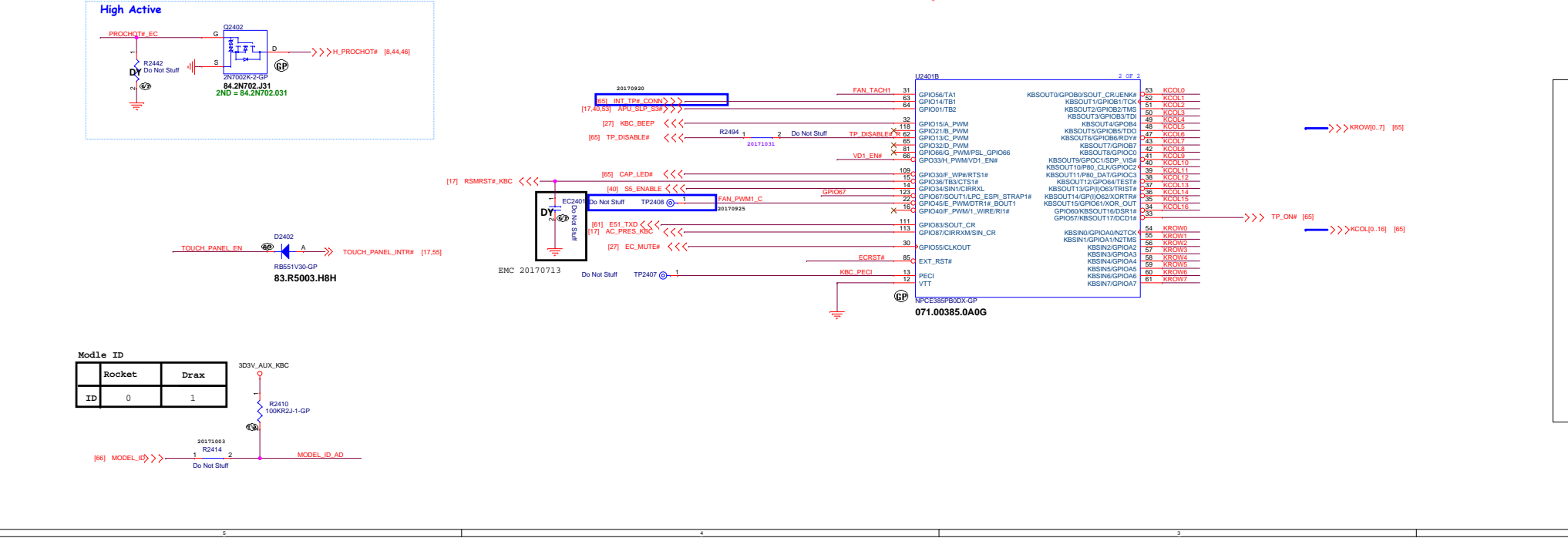
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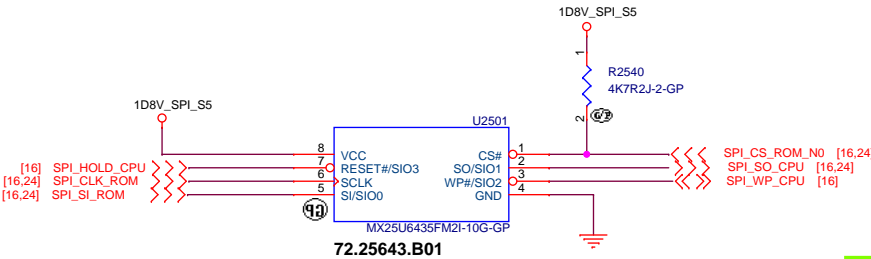
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SSID = KBC



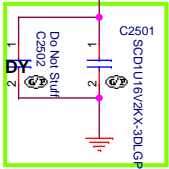
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for CPU

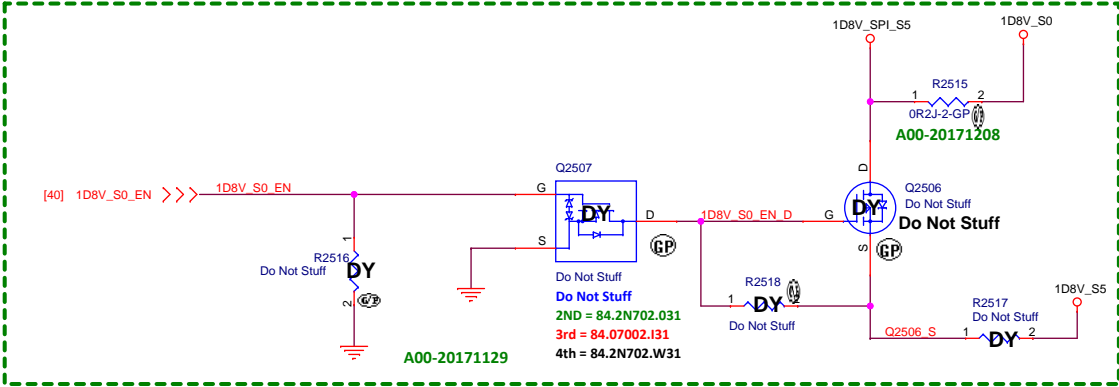


SPI ROM socket  
Co-Layout with U2501

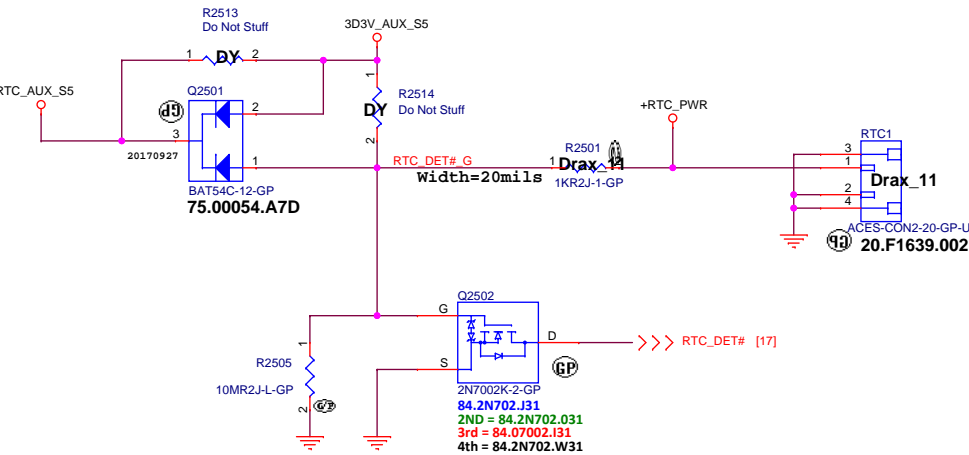
Remove SSKT1 co-lay  
A00-20171129



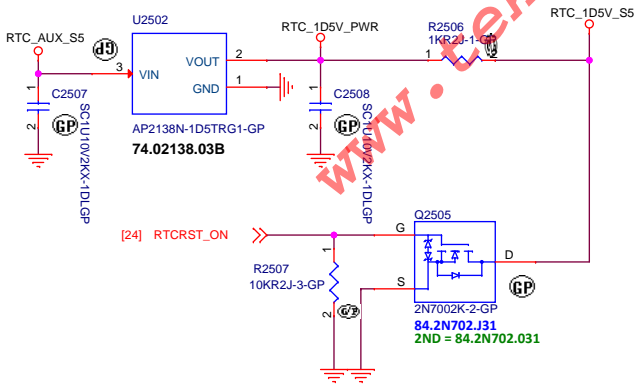
Layout Note: Close to U2501 Pin 8



SSID = RTC



Delete RTC2 Conn



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SSID = LOM

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A	B	C	D	E
SSID = LAN				
4				4
3				3
2				2
1				1
A	B	C	D	E

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SSID = LAN CONN

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Title <b>(Reserved)RJ45+Transformer</b>					
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SSID = USB

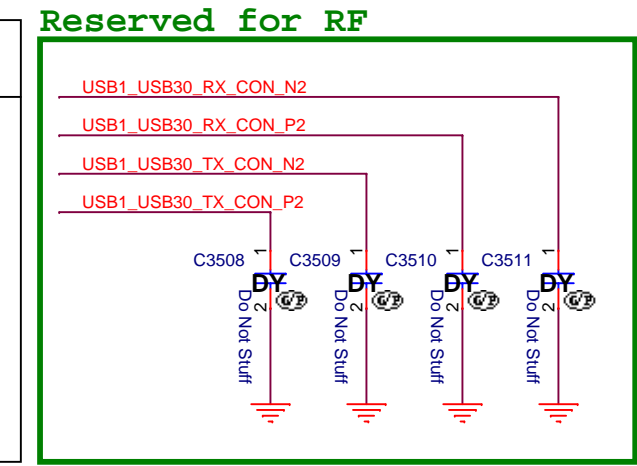
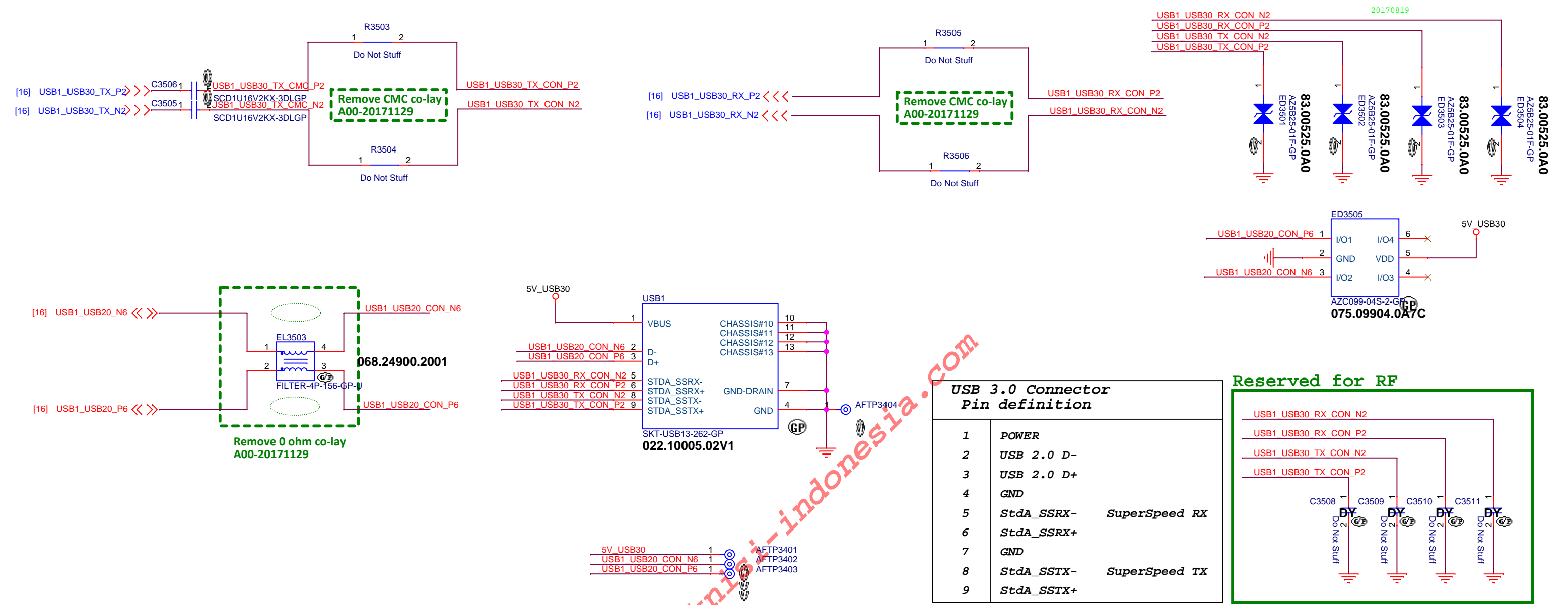
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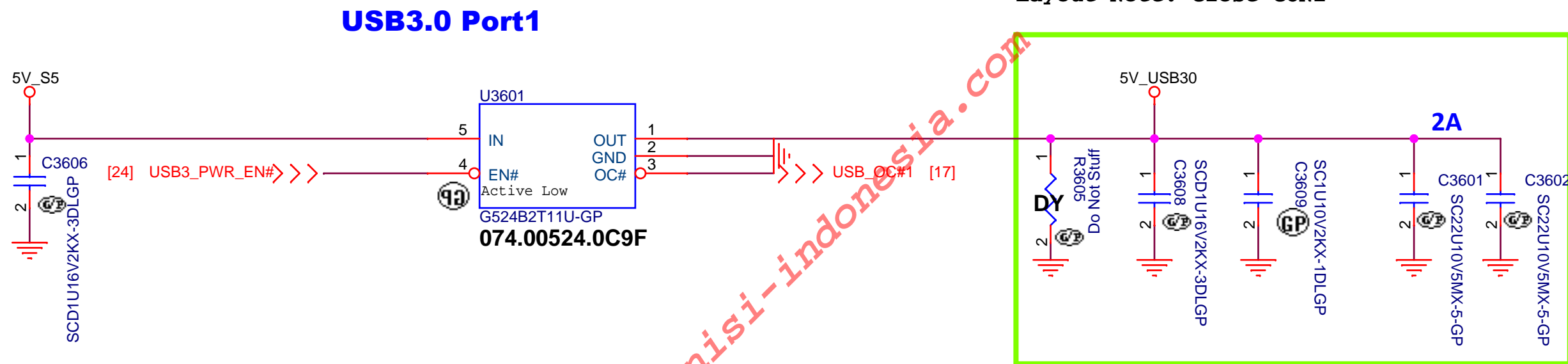
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Title <b><i>(Reserved)USB 2.0 Port</i></b>			
Size A4	Document Number <b><i>Drax MLK/Rocket MLK AMD</i></b>		Rev <b><i>A00</i></b>
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SSID = USB





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Title				<b>USB Power SW</b>					
Size	A4	Document Number			<b>Drax MLK/Rocket MLK AMD</b>			Rev	<b>A00</b>
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SSID = USB

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Title		
<b>USB2.0 HUB</b>		
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Drax Rocket MLK



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Title

**(Reserved)**

Size  
A4

Document Number

**Drax MLK/Rocket MLK AMD**

Rev

**A00**

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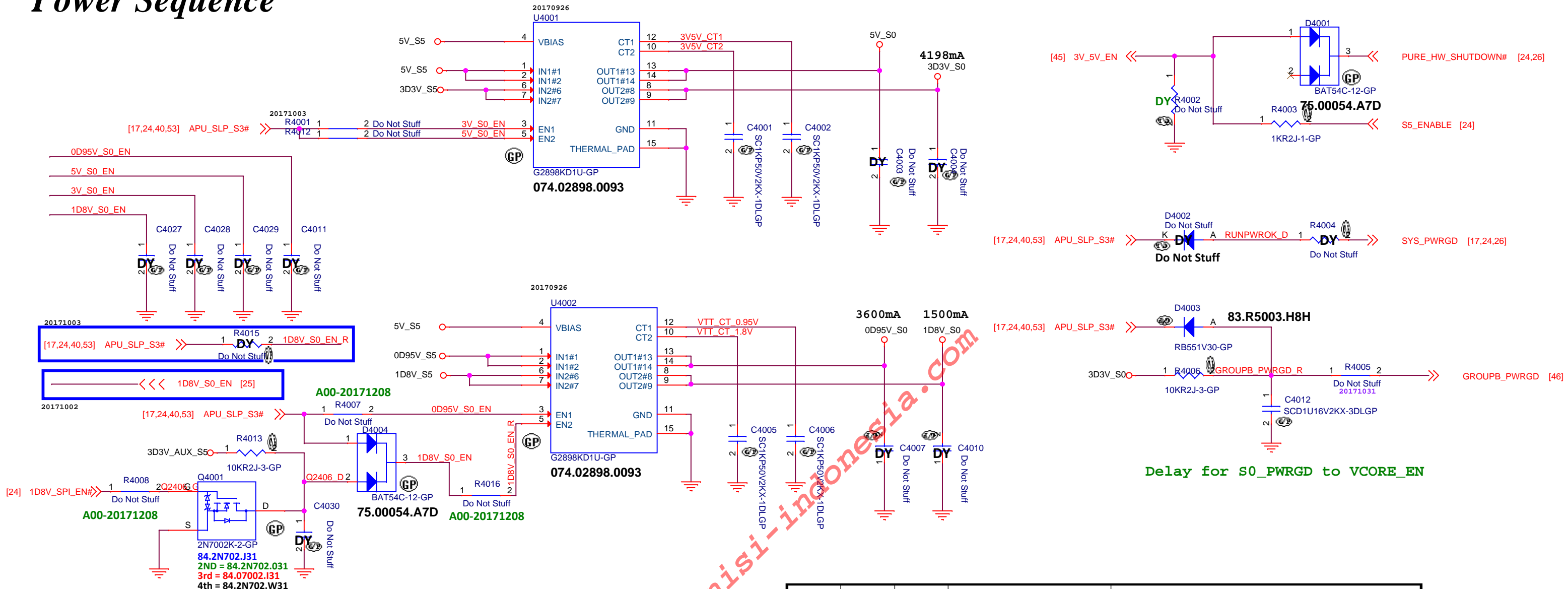
Blanking

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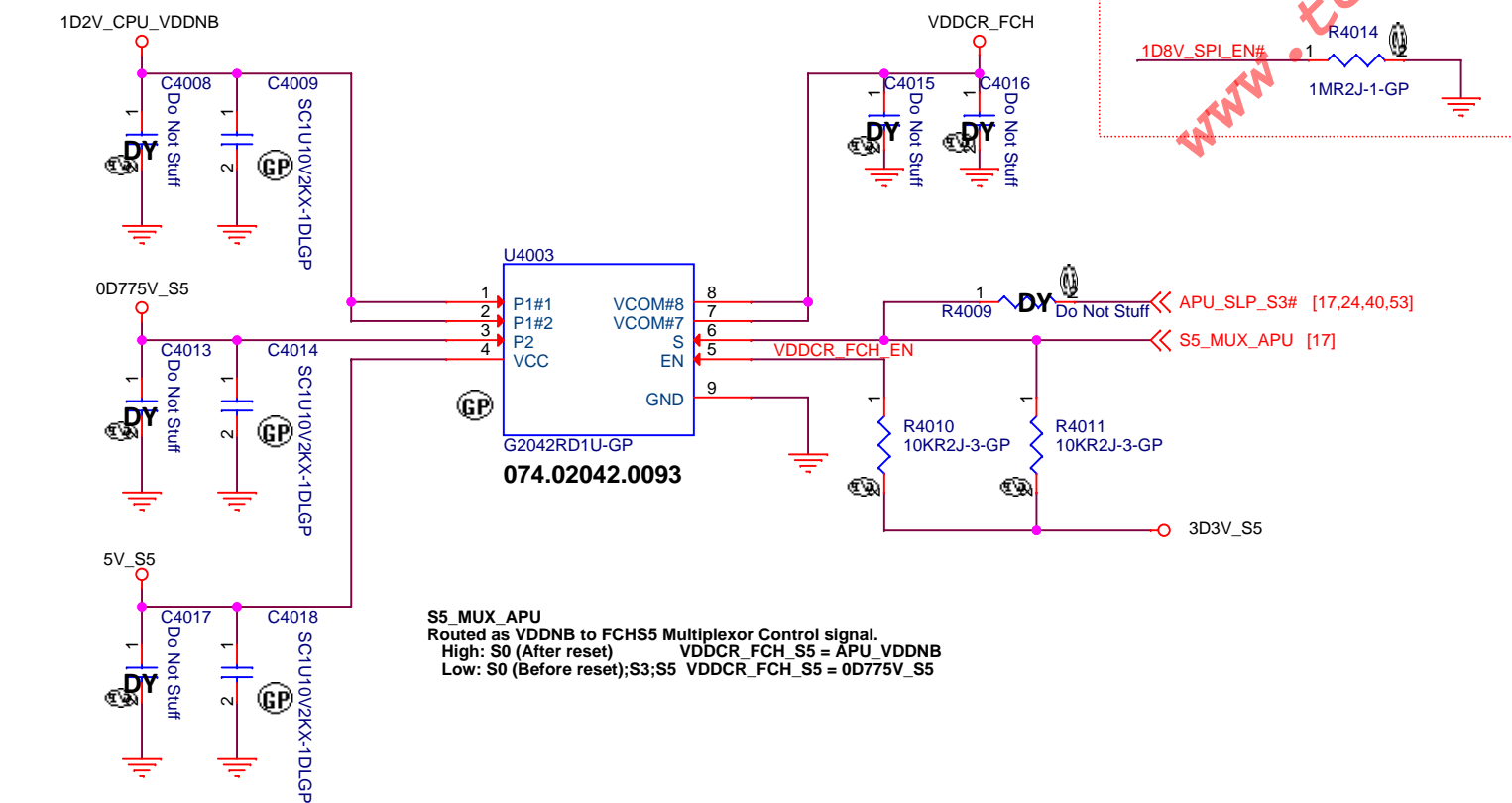
Drax Rocket MLK

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Power Sequence



VDDNB to FCHS5 Multiplexor Control signal



VCC	EN	S	P1 Voltage	Function
5	0	X	X	Both P1 and P2 do not pass to VCOM VCOM is with pull low R of 200 Ω
5	1	0	< P2	P2 passed to VCOM
5	1	0	> P2	P1 passed to VCOM
5	1	1	< 2.0V	P1 passed to VCOM

"X" means don't care

Table 148. S5\_MUX\_CTRL State Table

Platform Power State	S5_MUX_CTRL Signal Level	SLP_S3_L	SLP_S5_L	VDDCR_FCH_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON (= VDDCR_FCH_ALW)
S3	0	0	1	ON (= VDDCR_FCH_ALW)
S0, but still in Reset	0	1	1	ON (= VDDCR_FCH_ALW) or if VDDCR_NB ≥ VDDCR_FCH_ALW, tracks VDDCR_NB
S0	1	1	1	Tracks VDDCR_NB

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Title

**Power Plane Enable&Sequence**


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Date: Tuesday, January 02, 2018		Sheet 40 of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

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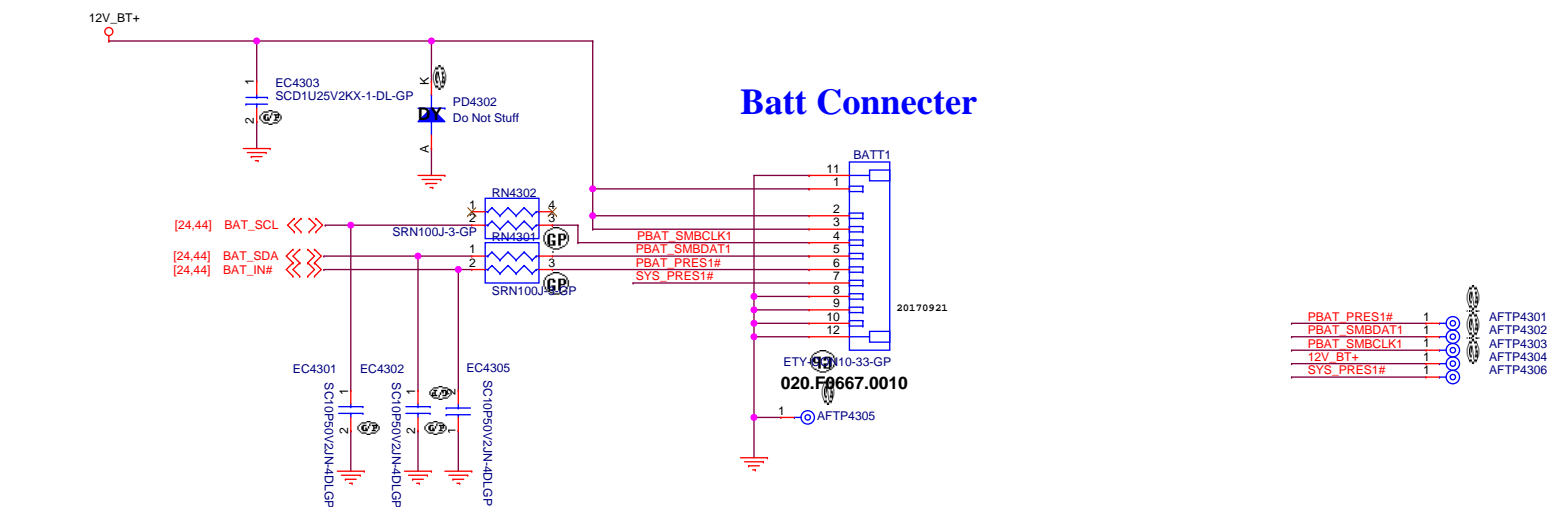


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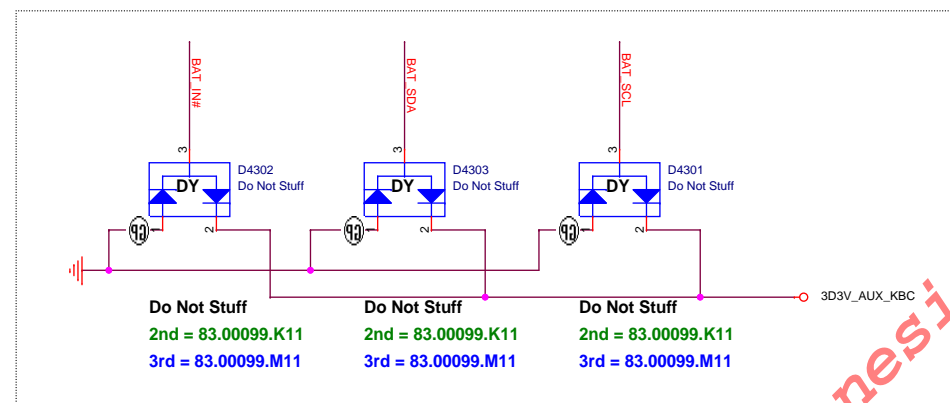
Title (Reserved)

Size A4	Document Number <b>Drax MLK/Rocket MLK AMD</b>	Rev <b>A00</b>
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```
SSID = PWR.Support
```



Placement: Close to Batt Connector

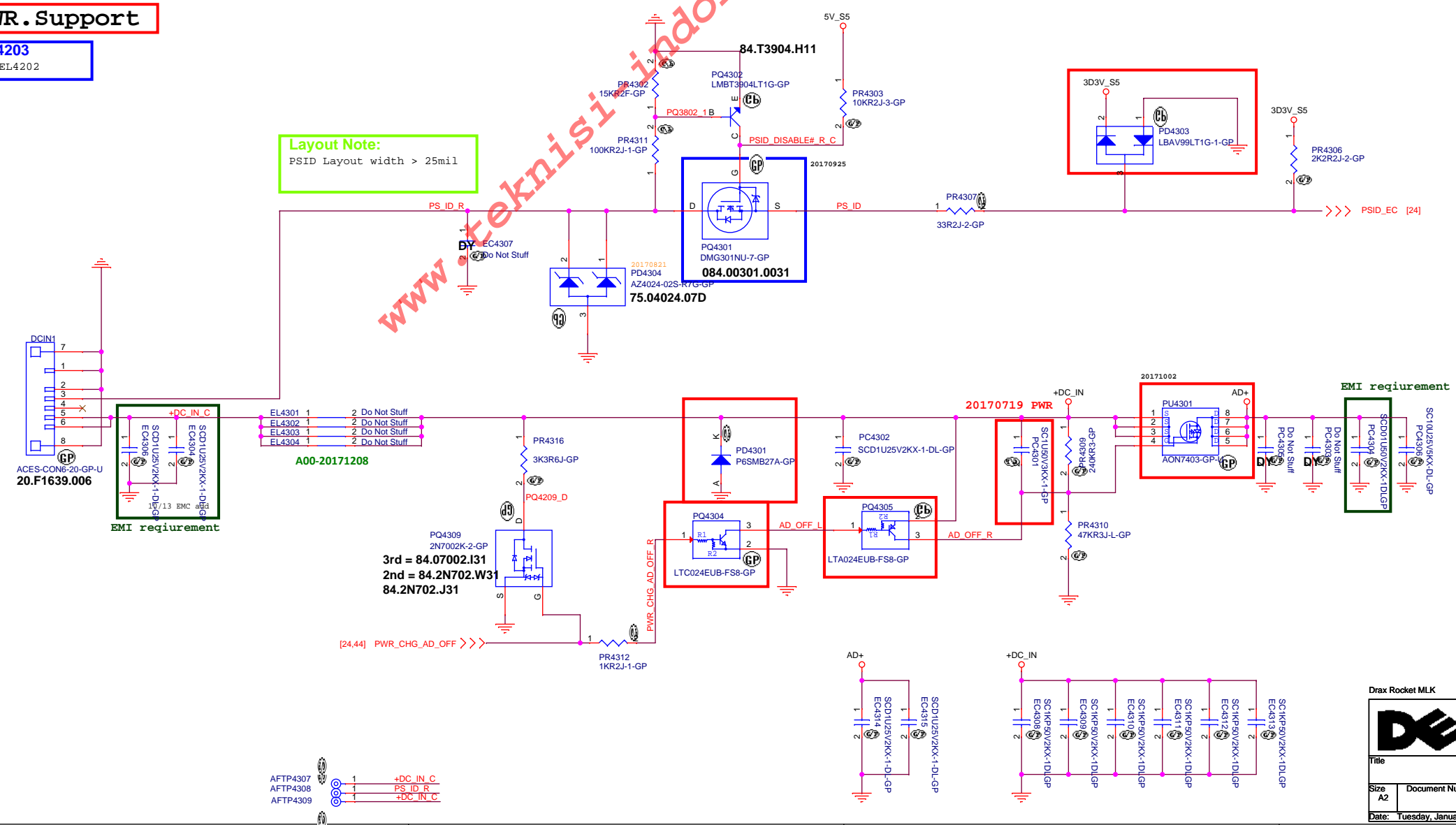


```
SSID = PWR.Support
```

**0103 Add EC4203**  
ndde close to EL4202

ndde close to EL4202

**Layout Note:**  
PSID Layout width > 25mil



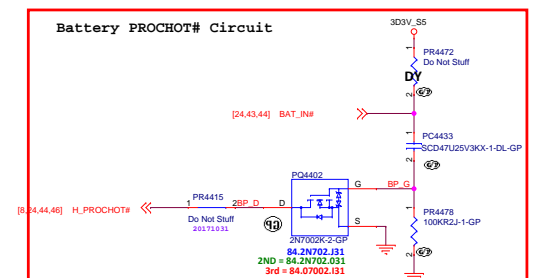
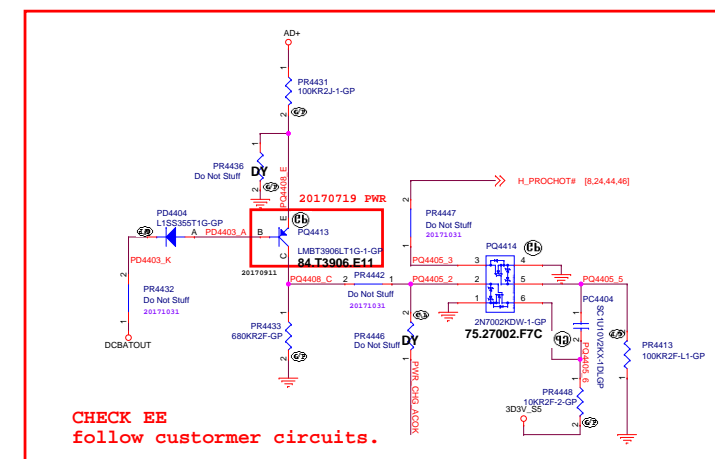
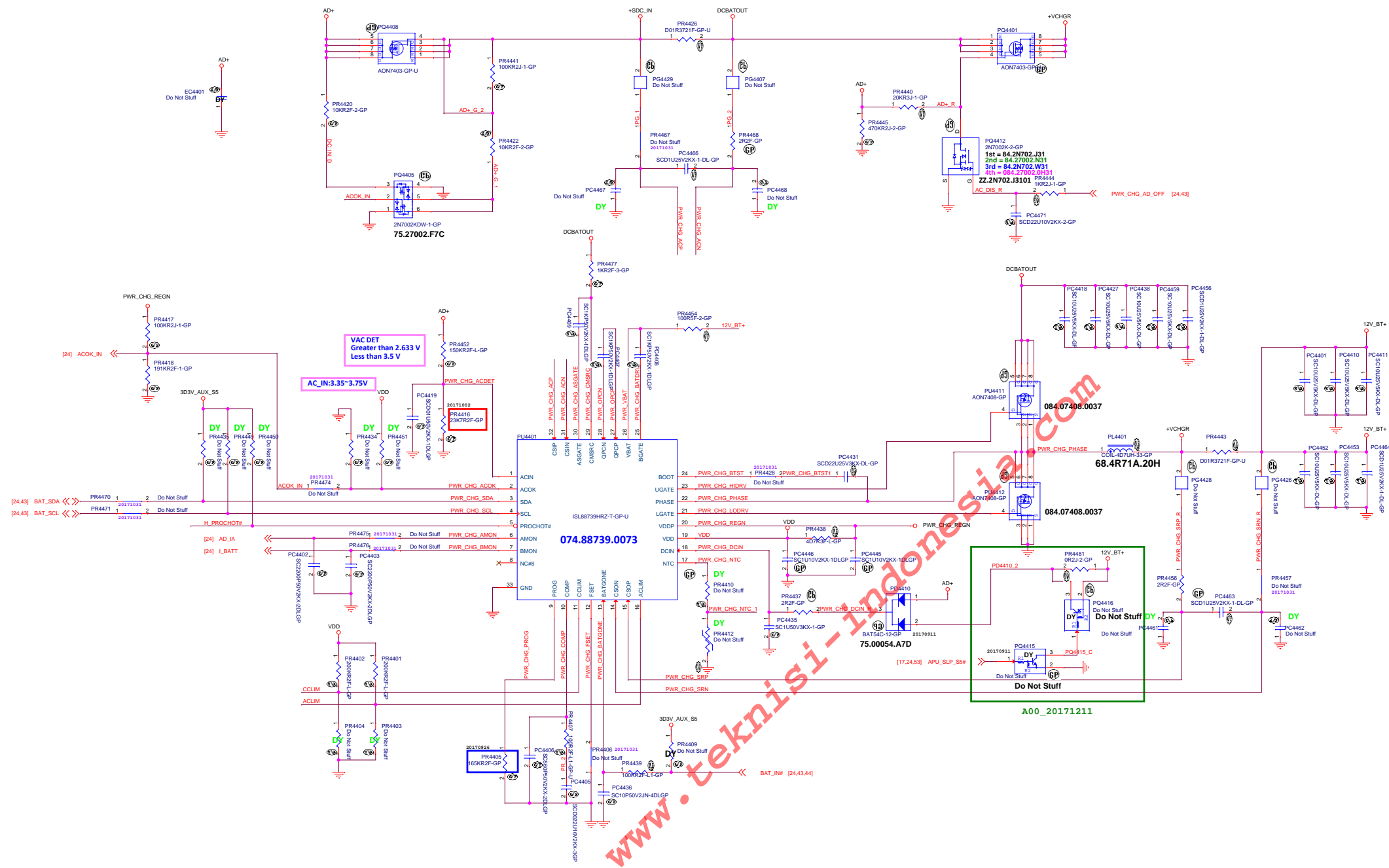
Drax Rocket MLK



Title			
<b>BATTERY CONN</b>			
Size A2	Document Number	Rev	
	<b>Drax MLK/Rocket MLK AMD</b>	<b>A00</b>	
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Main Func = Charger



CHECK EE  
follow customer circuits.

```
SSID = PWR.Plane.Regulator_5v3p3v
```

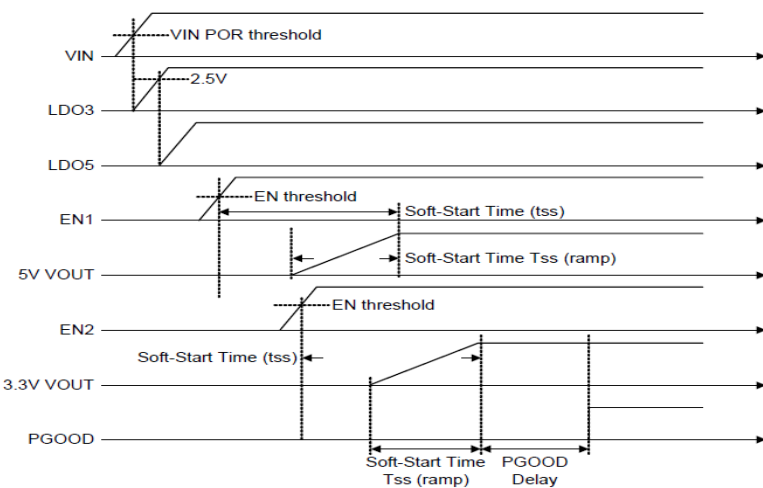
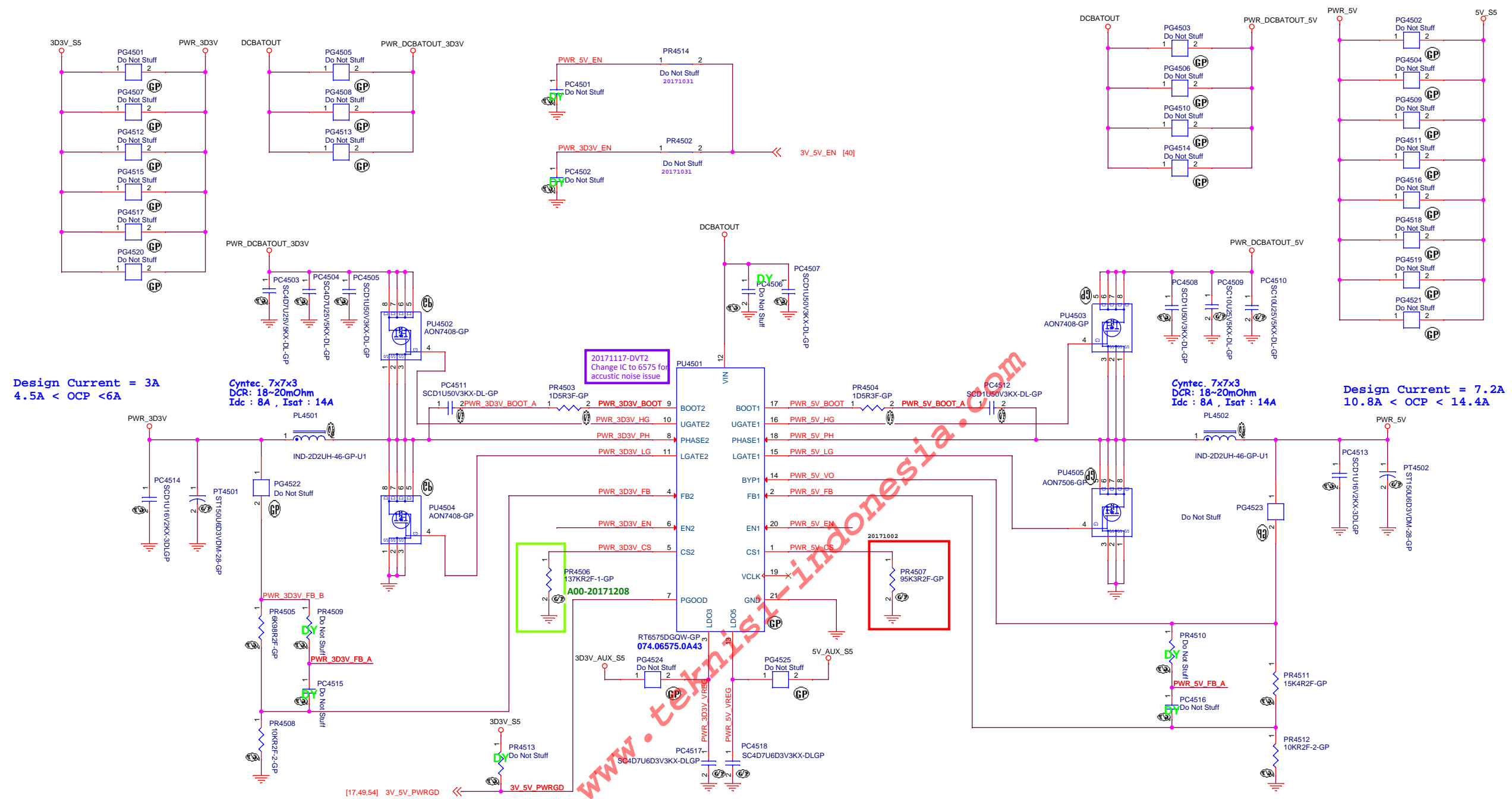
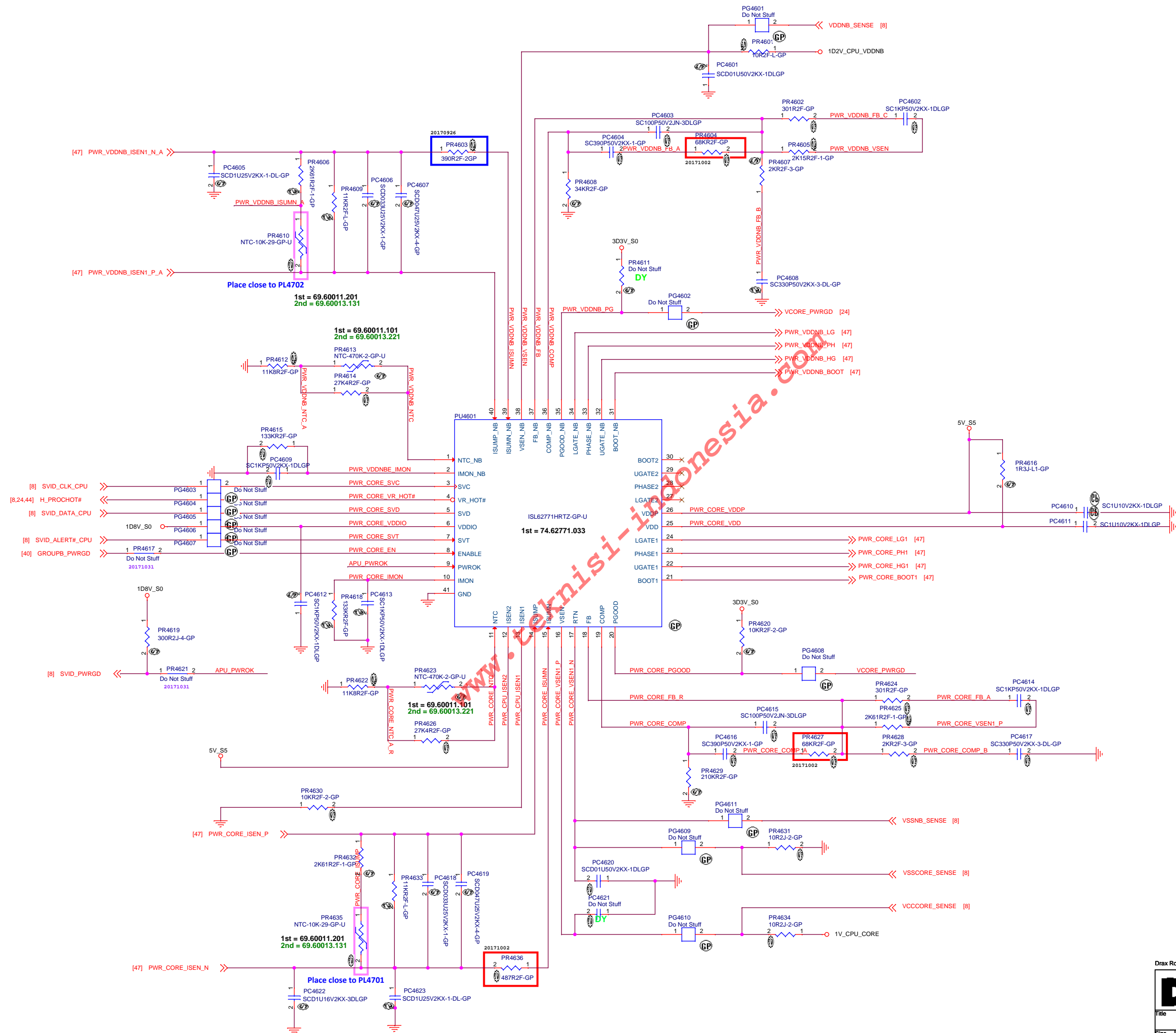
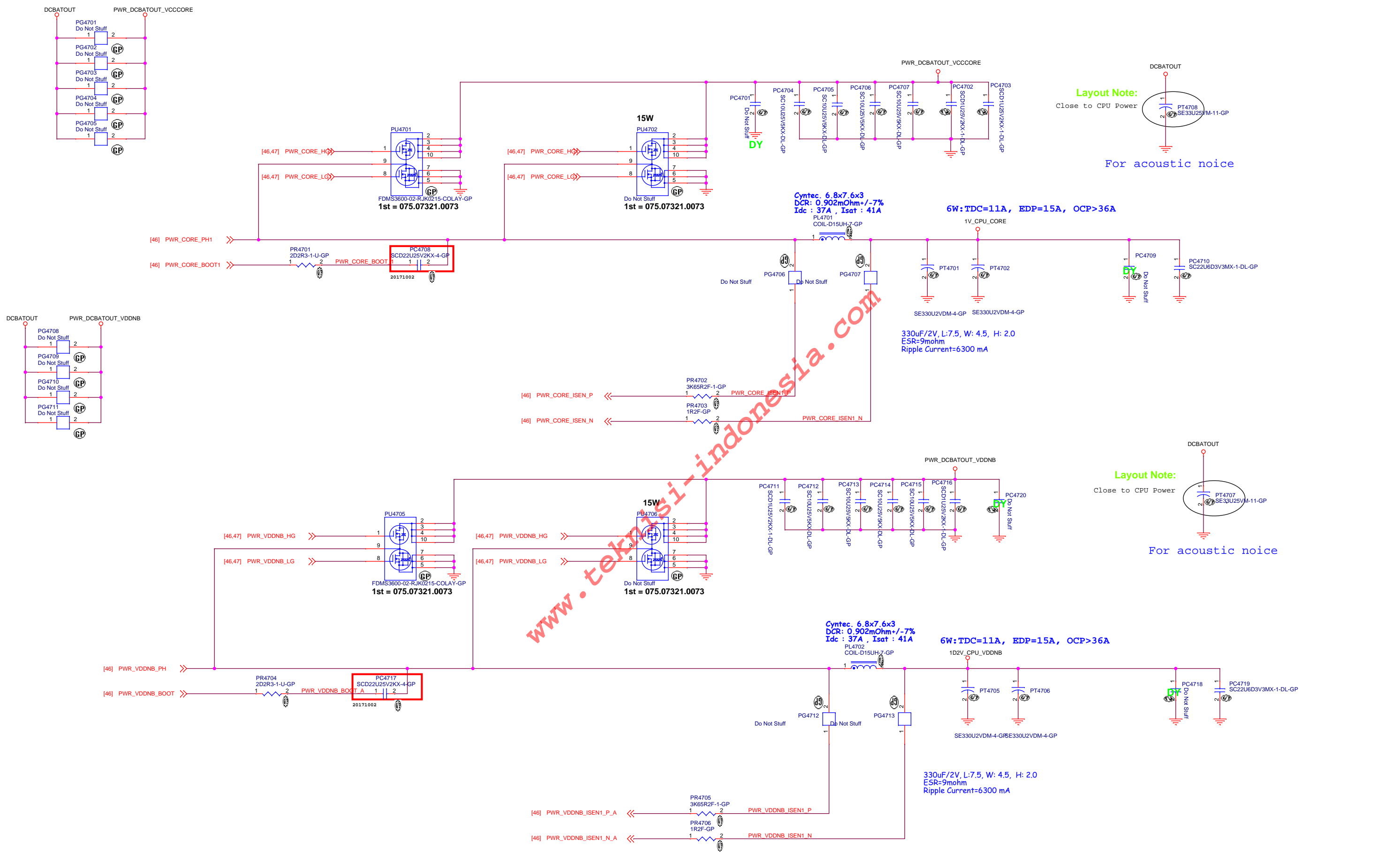


Figure 6. RT6575B Timing

```
SSID = CPU.Regulator
```



SSID = CPU.Regulator



Layout Note:  
Close to CPU Power

For acoustic noise

Layout Note:  
Close to CPU Power


For acoustic noise

5	4	3	2	1
D				D
C				C
B				B
A				A

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5	4	3	2	1
D				D
C				C
B				B
A				A

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5	4	3	2	1
D				D
C				C
B				B
A				A

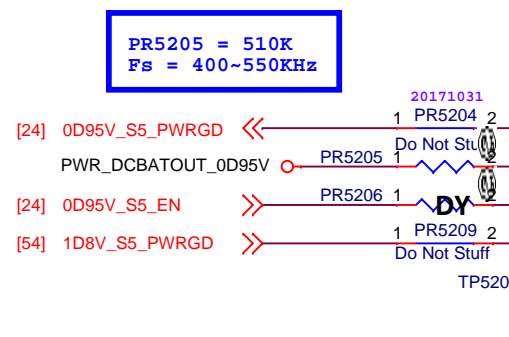
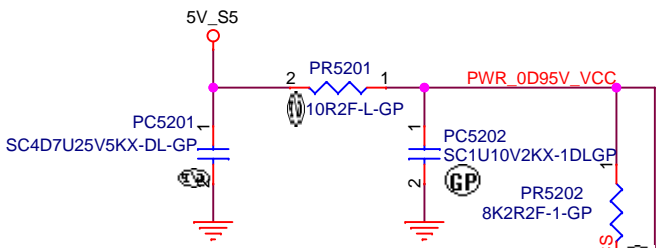
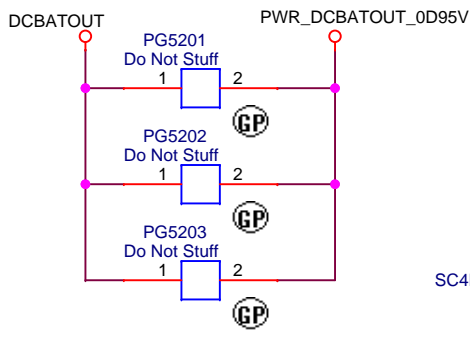
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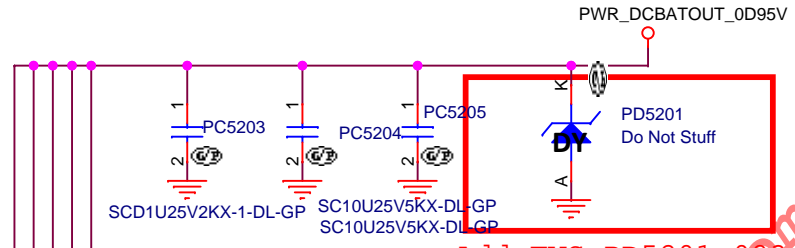
Drax Rocket MLK

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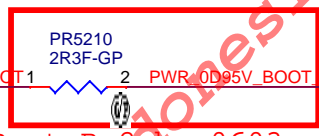




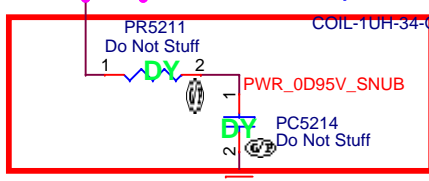
PR5205 = 510K  
Fs = 400~550KHz



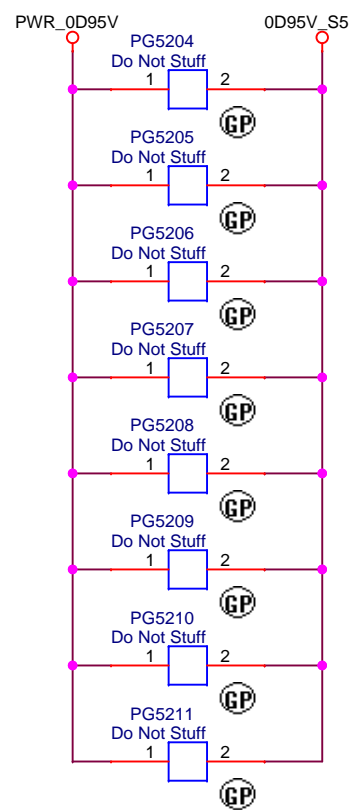
Add TVS PD5201 083.04024.0AA1



Add Boot R 20ohm 0603 and Net name

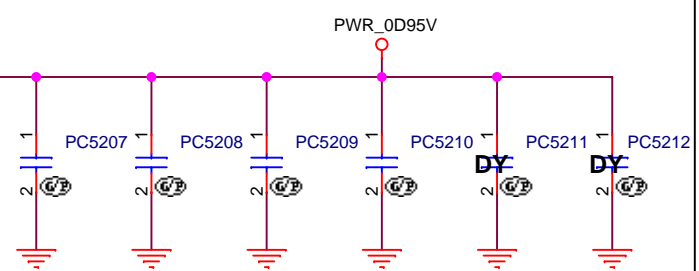


Add DY RC snubber and Net name  
2.2 ohm 0805  
1000 pF 0402 50V



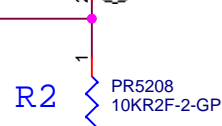
TDC : 7.69A  
15.38A > OCP > 11.535A

Cyntec. 7 x 7 x 3.0 mm  
DCR: 9m~10mOhm  
Idc : 11 A , Isat : 22A



Manual: 64.40215.6DL for 25W

$$V_{out} = 0.75 * (1 + R1/R2) = 0.95V$$



Drax Rocket MLK

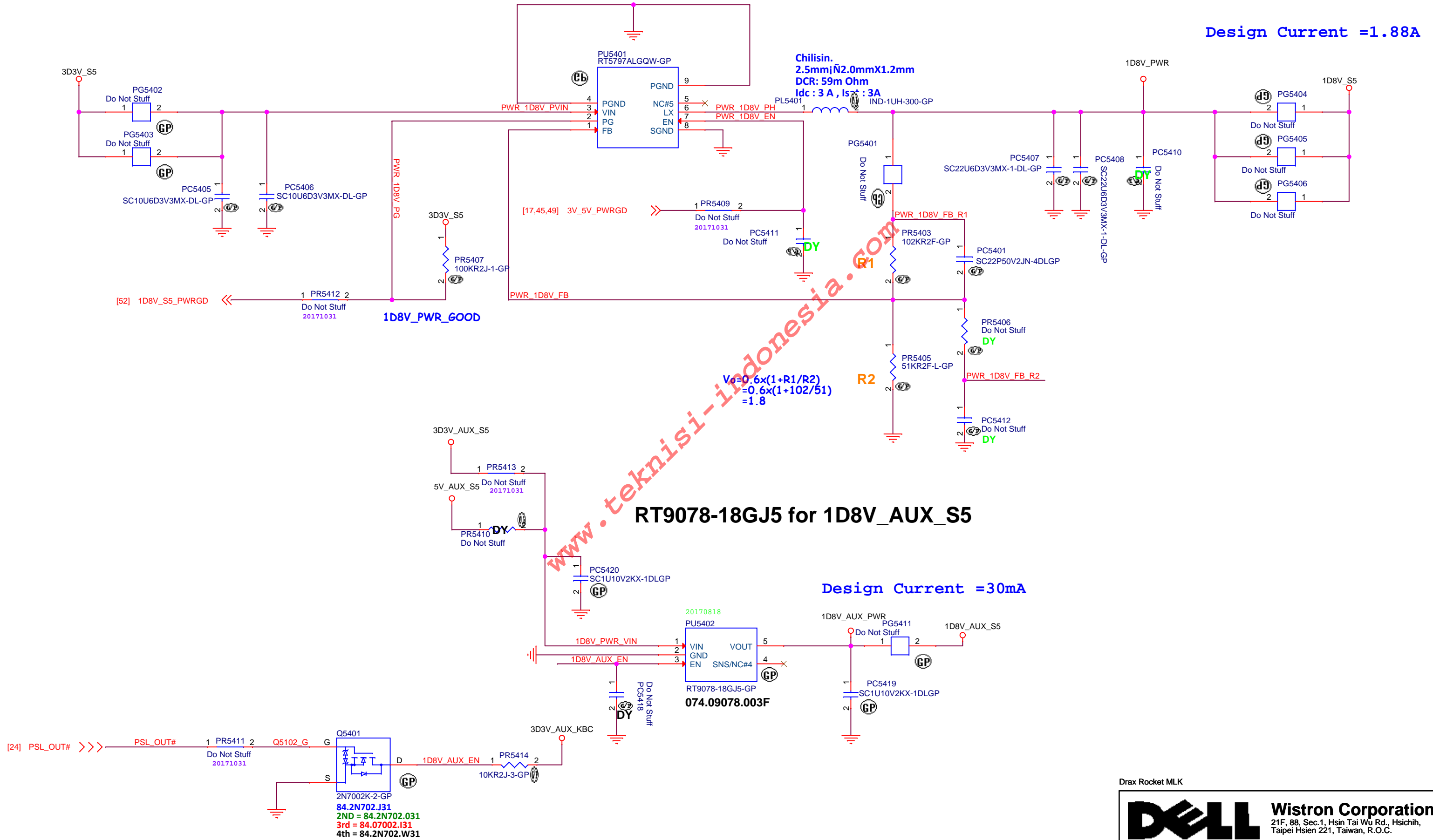


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Title <b>G5338K11U_0D95V</b>		
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```
SSID = PWR.Plane.Regulator_1p5v_1p8v
```



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Title
-------

**DC2DC\_1D8V/1D5V(RT5797)**

Size  
A3

Document Number  
**Drax MLK/Rocket MLK AMD**

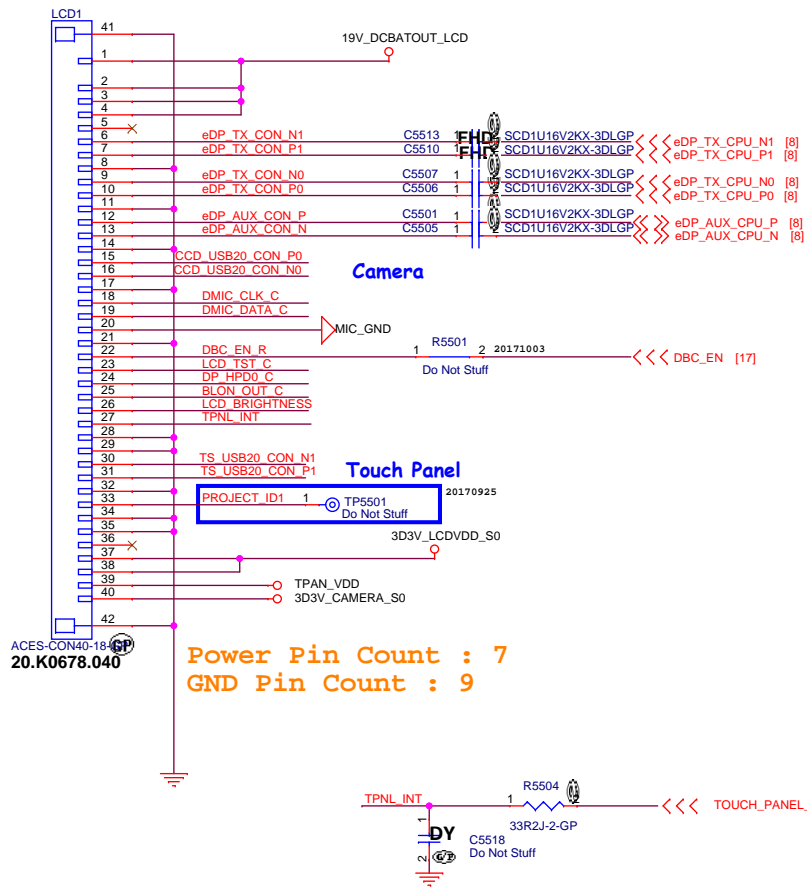
Rev  
**400**

Date: Tuesday, January 02, 2018

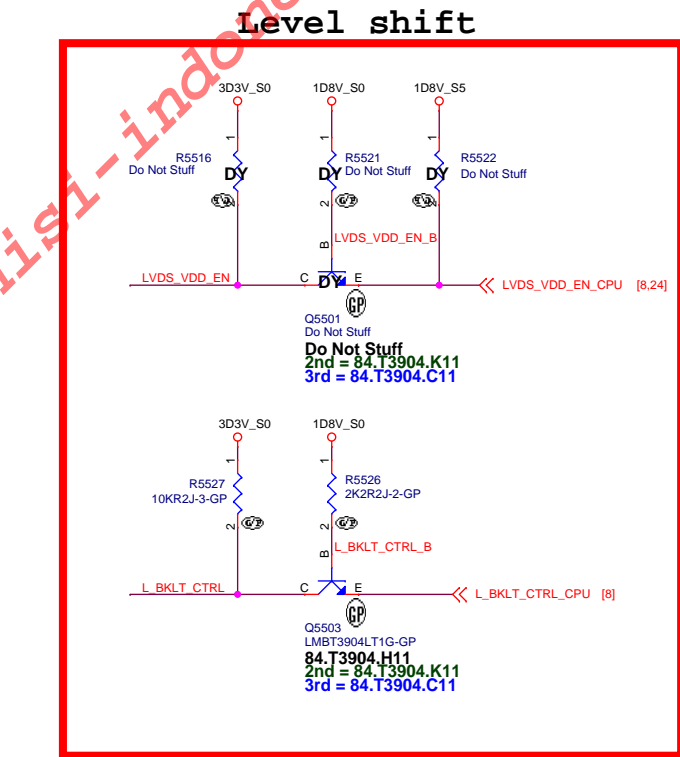
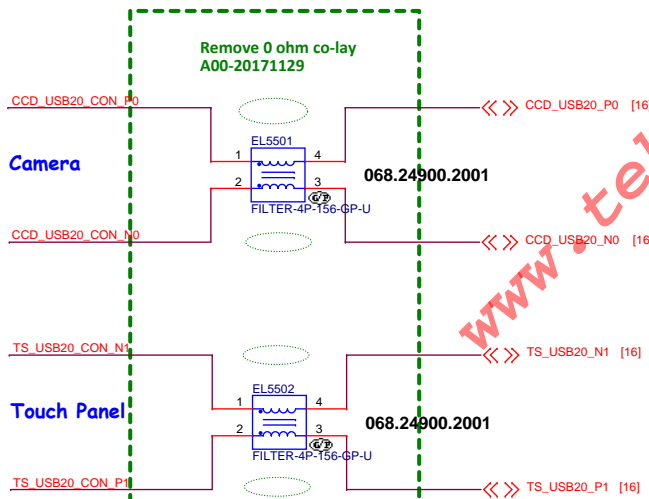
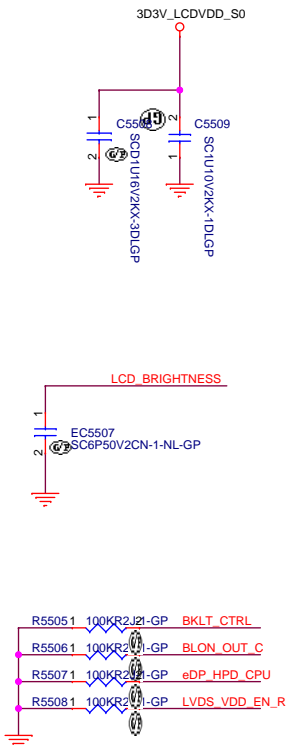
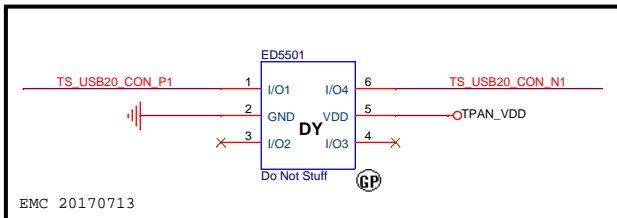
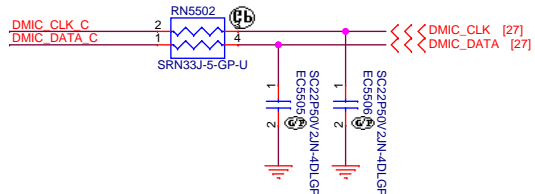
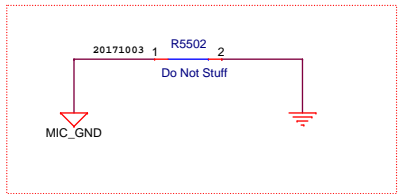
Sheet 54 of 106

SSID = VIDEO

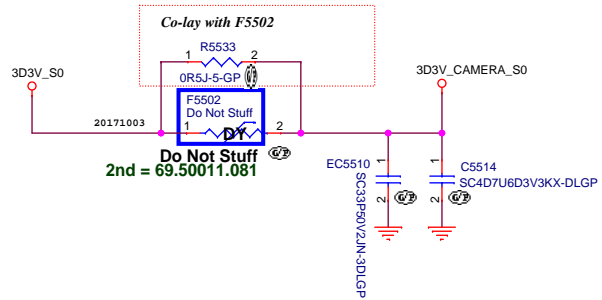
## Panel Conn.



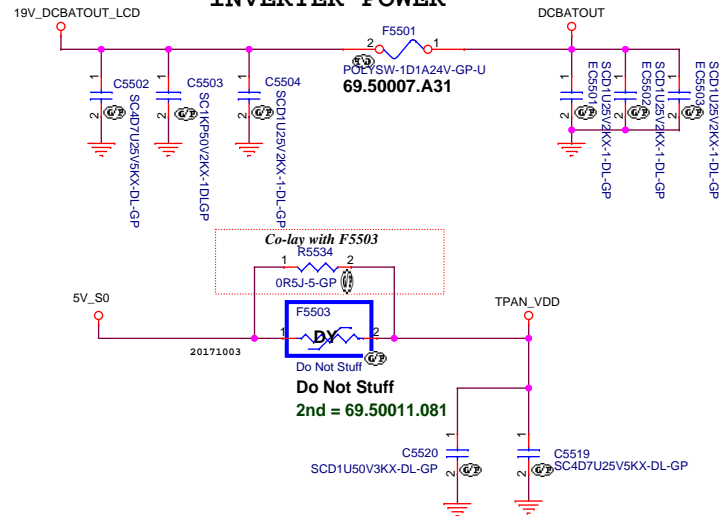
Layout: Close CONN LCD1



## CAMERA POWER



## INVERTER POWER



Drax Rocket MLK

**DELL** Wistron Corporation  
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Title: LCD Connector  
Size: A2 Document Number: Drax MLK/Rocket MLK AMD Rev: A00  
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SSID = Display Port

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Title <b>(Reserved) Display Port</b>					
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SSID = DVI

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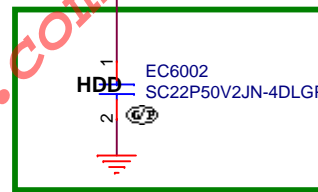
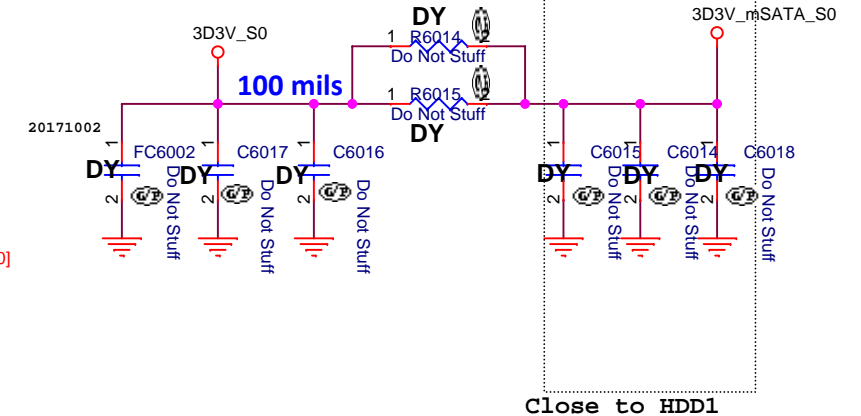
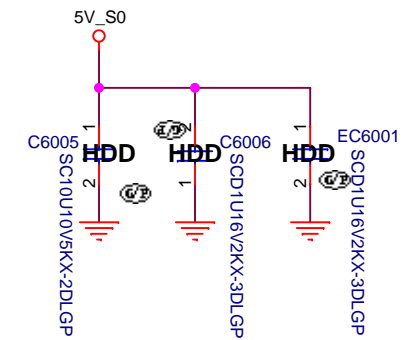
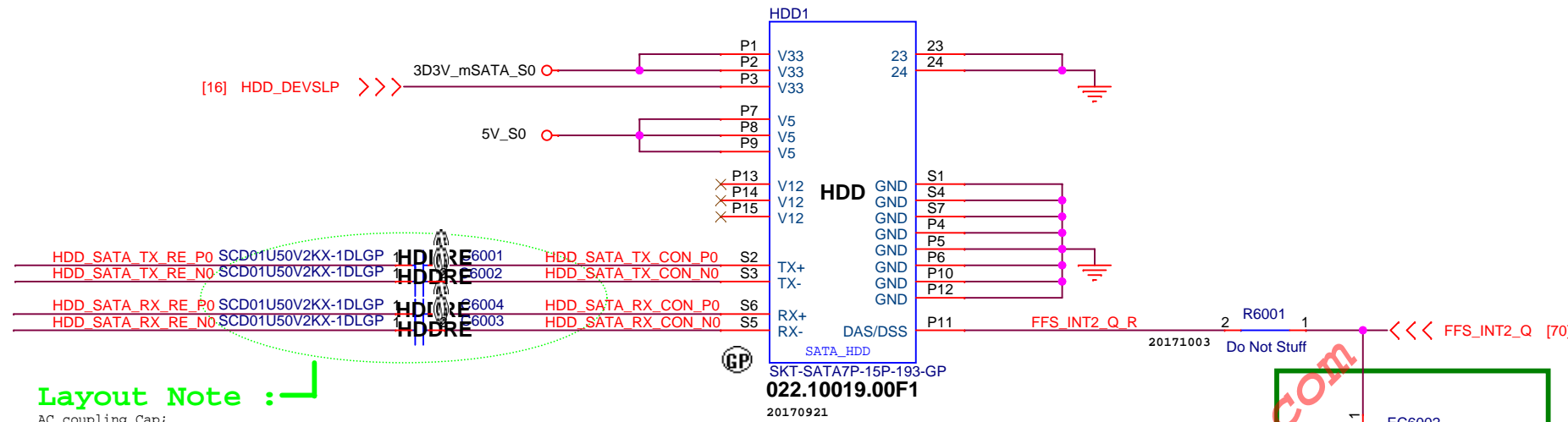
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Title <b>(Reserved) DVI</b>					
Size	Document Number <b>Drax MLK/Rocket MLK AMD</b>				Rev <b>A00</b>
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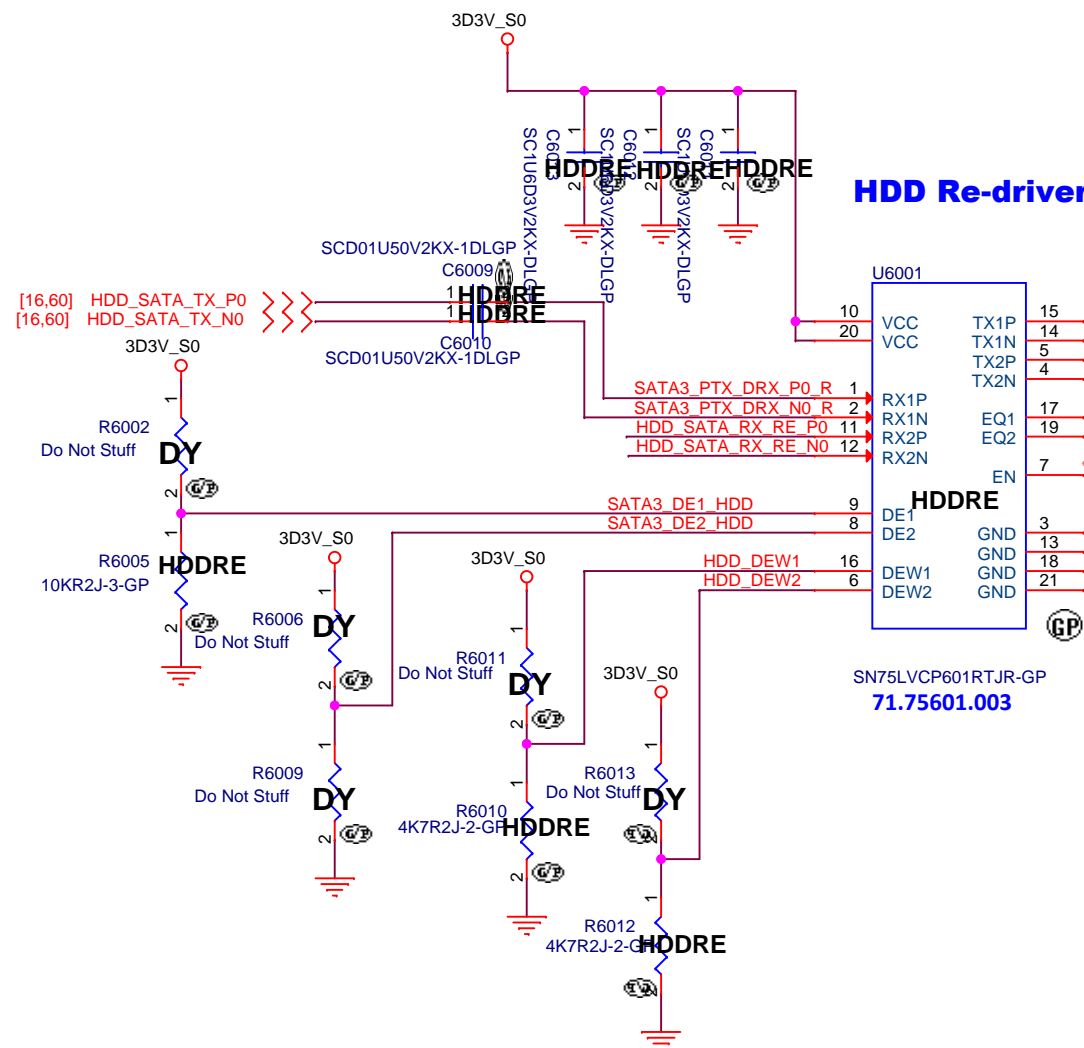
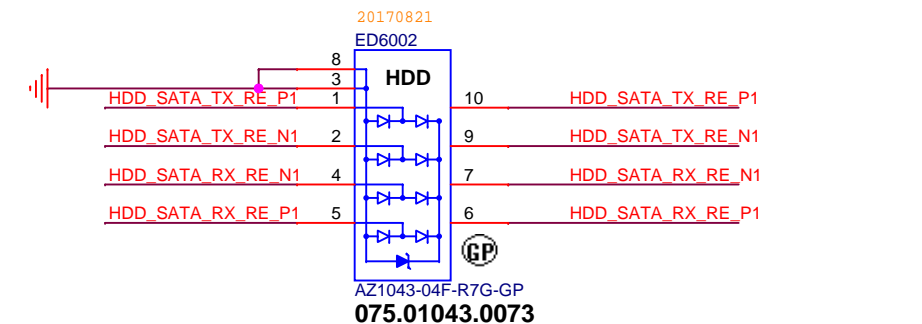
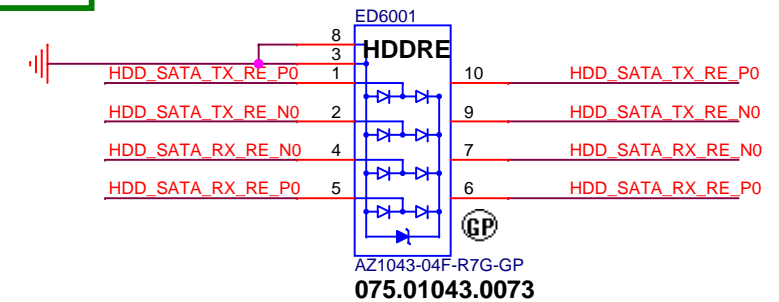


SSID = SATA

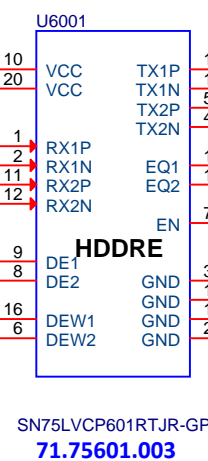
# SATA HDD Connector



EMC Request  
A00-20171208



HDD Re-driver

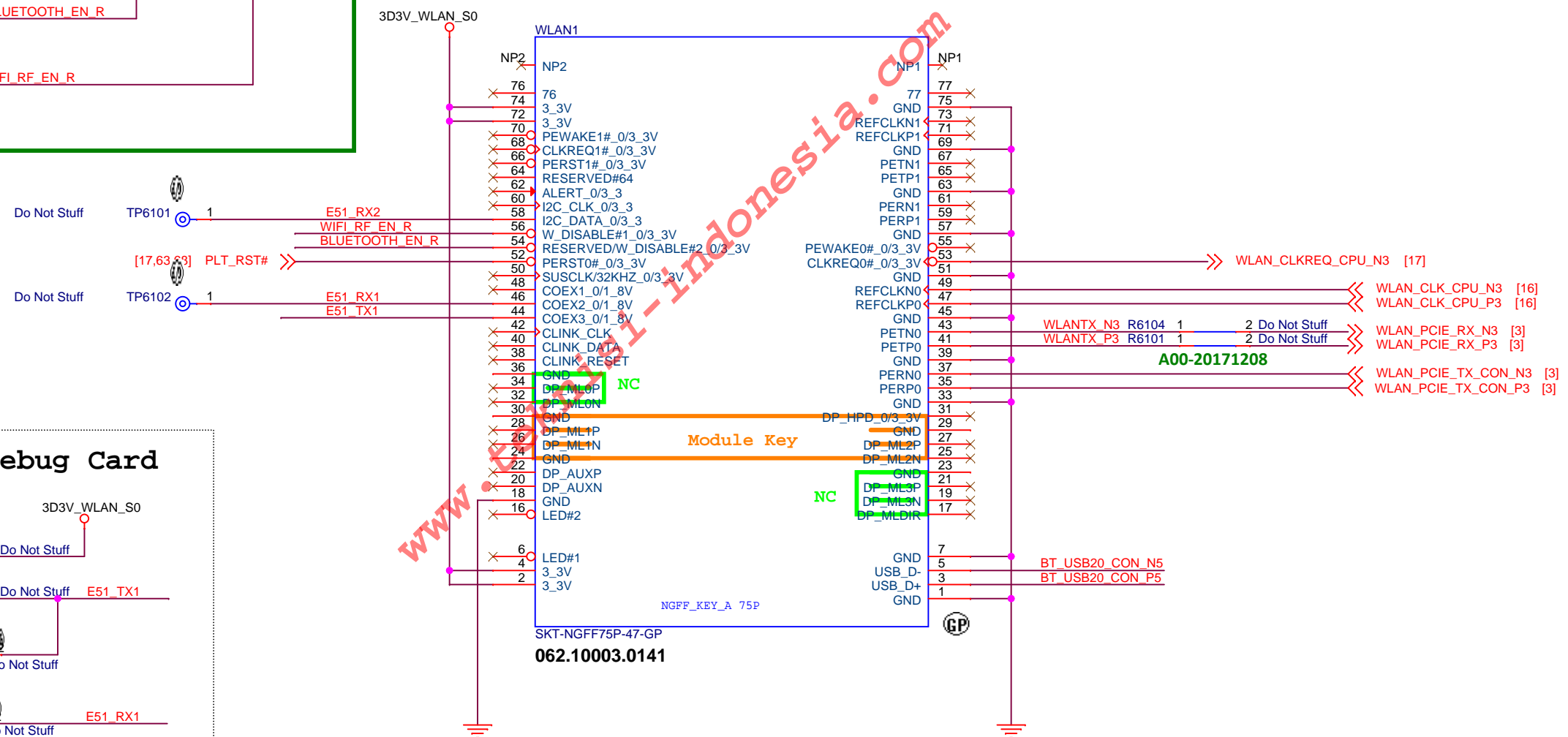
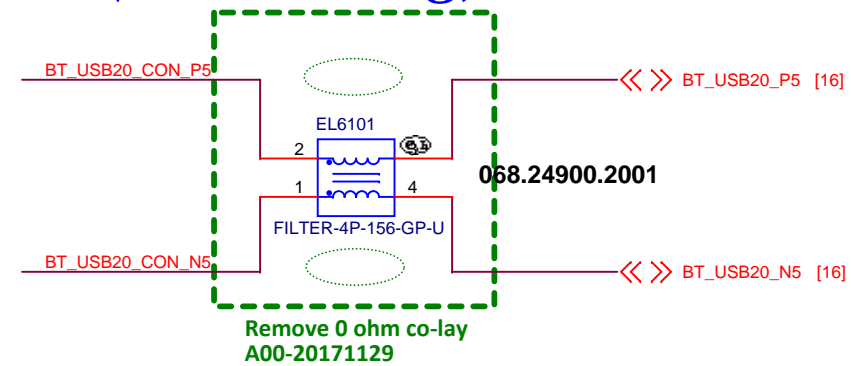
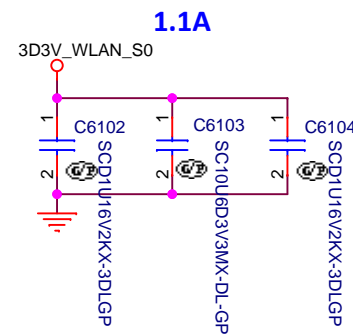
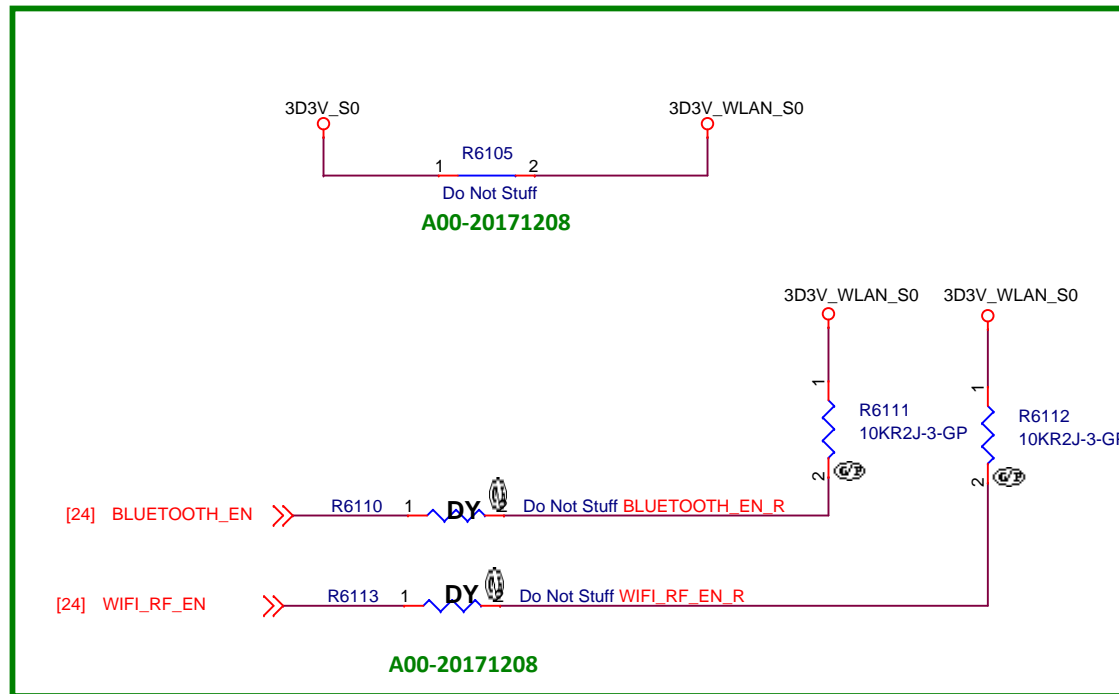


Drax Rocket MLK

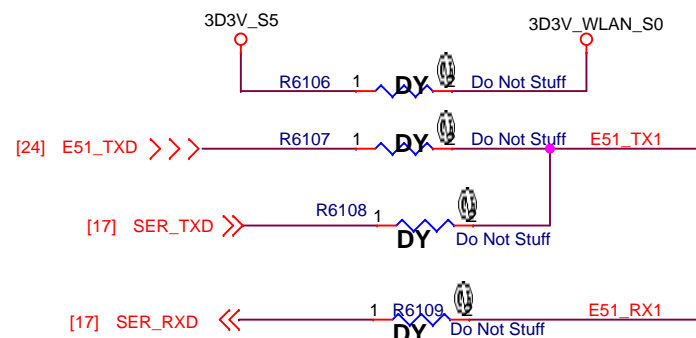


SSID = WLAN

## Mini Card Connector(802.11a/b/g)



### Reserved for NGFF Debug Card



EE Note:  
For NFGG Debug Card:  
Stuff R6106,R6107,R6108(optional).  
DY R6105

3D3V_WLAN_S0	1	AFTP6101
WLAN_CLKREQ_CPU_N3	1	AFTP6102
WIFI_RF_EN	1	AFTP6104
PLT_RST#	1	AFTP6105
BLUETOOTH_EN	1	AFTP6110
BT_USB20_CON_N5	1	AFTP6111
BT_USB20_CON_P5	1	AFTP6113

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Title  
**WLAN**

Size Document Number  
**Drax MLK/Rocket MLK AMD**

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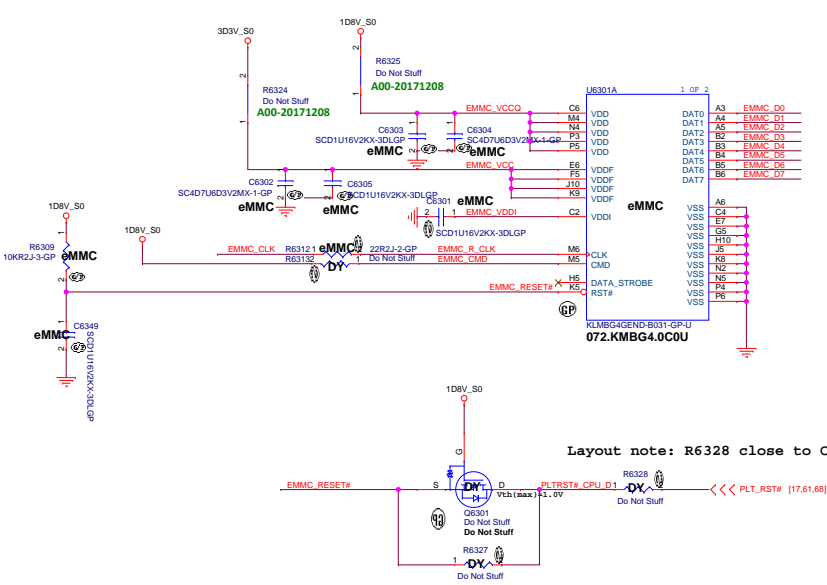
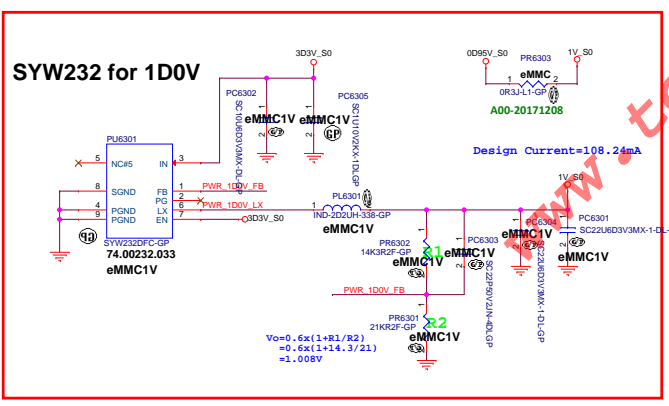
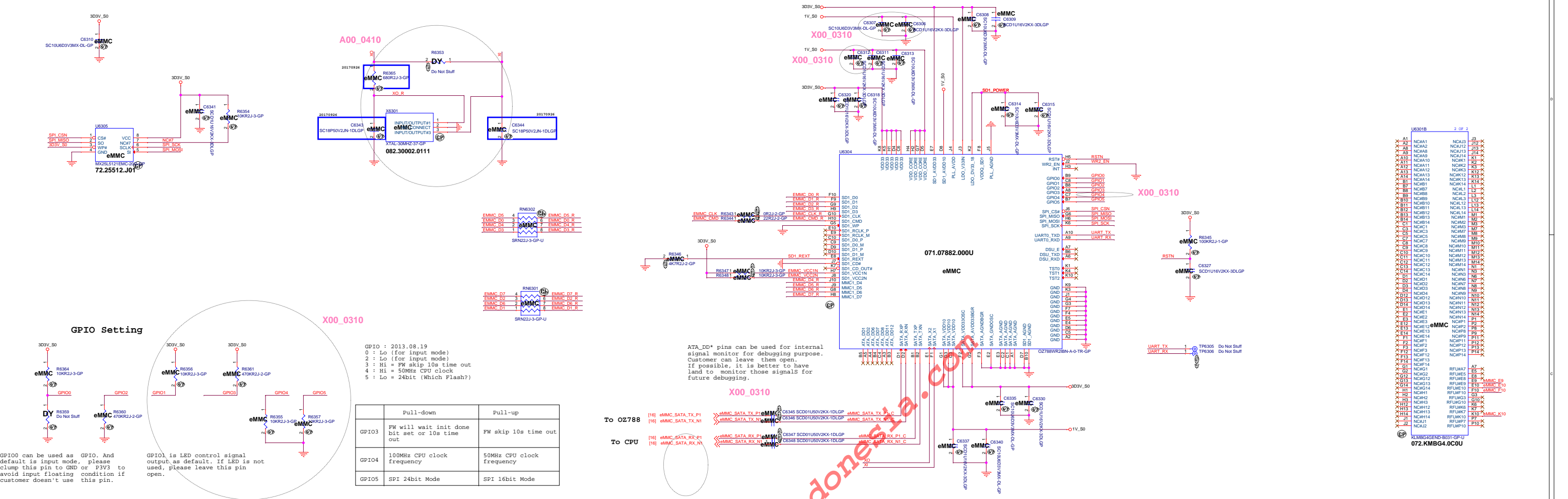
SSID = WWAN

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Title <b>(Reserved) WWAN</b>		
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	SKU1	SKU1.1	SKU2	SKU3
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4V	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4V	BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4T	BRASWELL 4c FCBGA 1.6GHz 6W, GT 16EU, CELERON Q3 Q4S
eMMC	Hynix/32G	Hynix/32G	SanDisk/32G	Samsung/32G
	SKU7	SKU8	SKU9	
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4V	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4V	BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON Q3 Q4T	
eMMC	Hynix/64G	SanDisk/64G	Samsung/64G	

5	4	3	2	1
SSID = LED / PWRBTN				
D				D
C				C
B				B
A				A
5	4	3	2	1

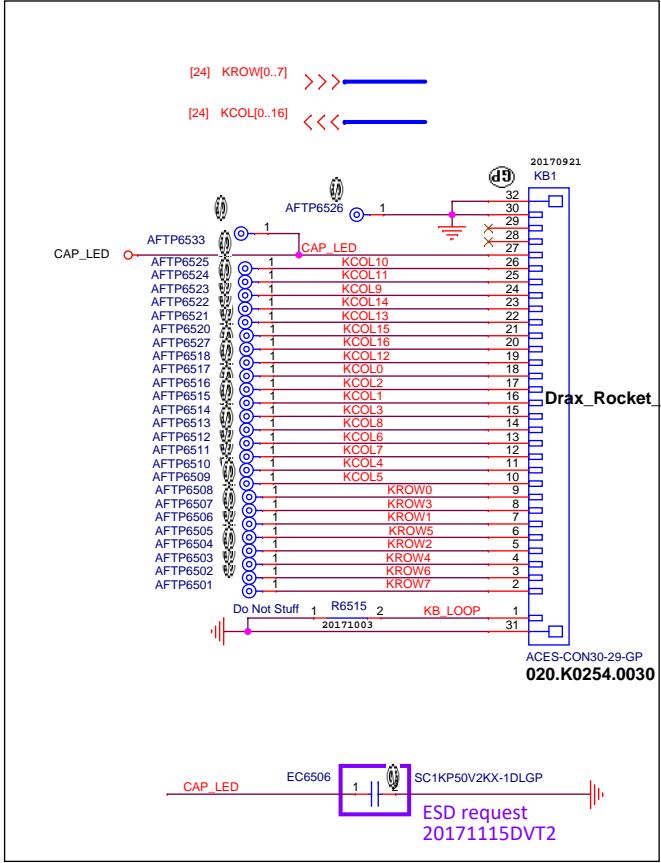
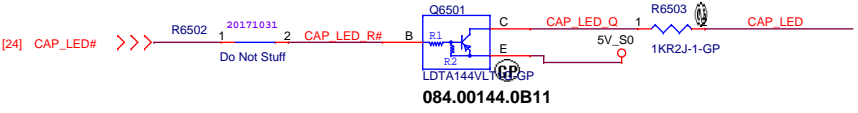
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Title <b><i>LED / PWRBTN</i></b>			
Size A4	Document Number <b><i>Drax MLK/Rocket MLK AMD</i></b>		Rev <b><i>A00</i></b>
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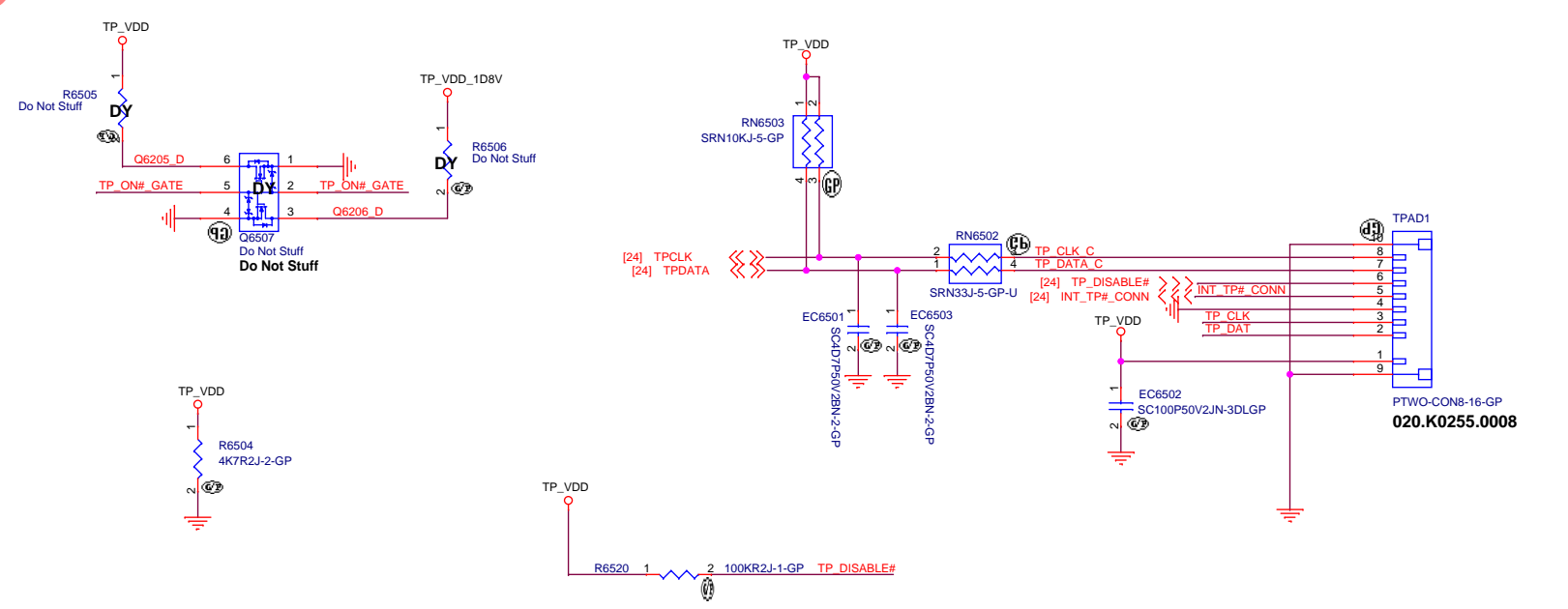
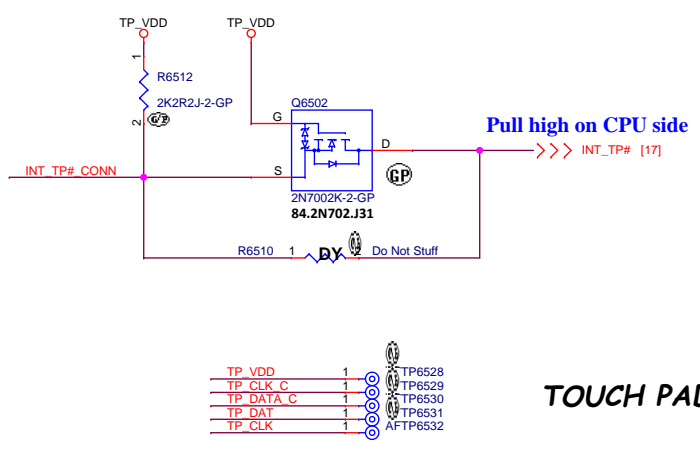
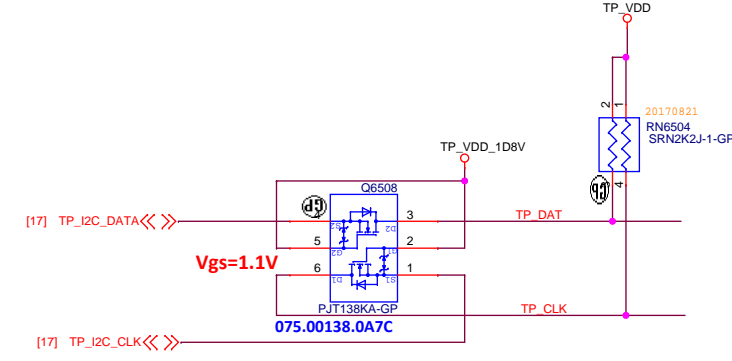
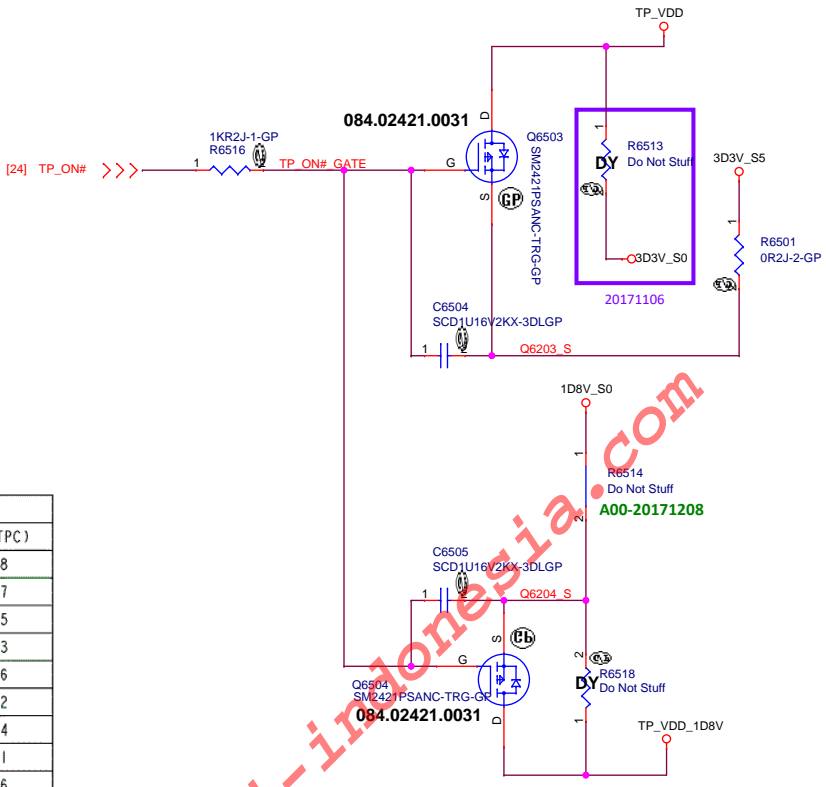
SSID = KB / TOUCH PAD

**CAP LED Control**  
LOW acted from KBC GPIO

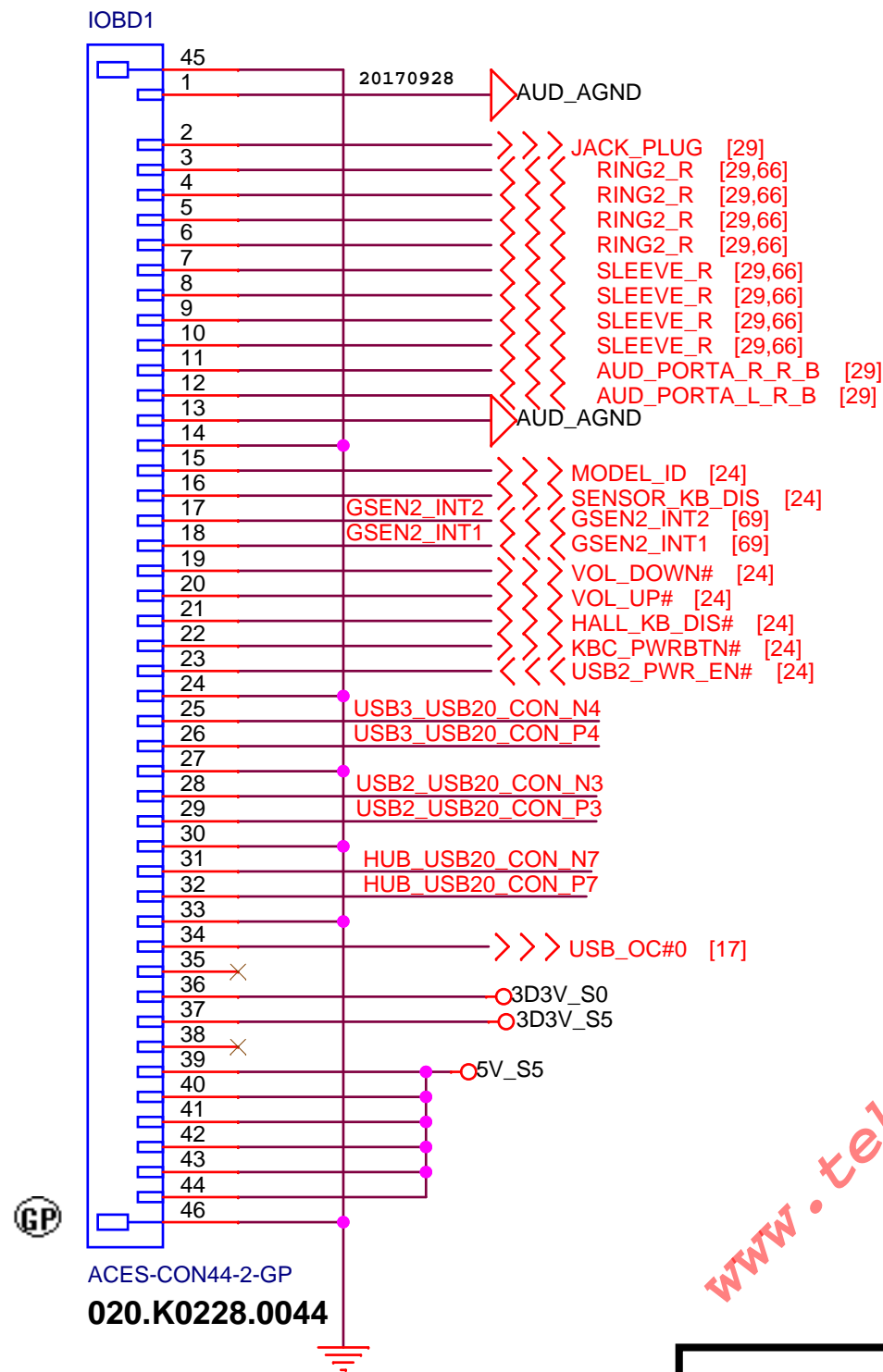


20170925  
**Delete KB2 Conn**

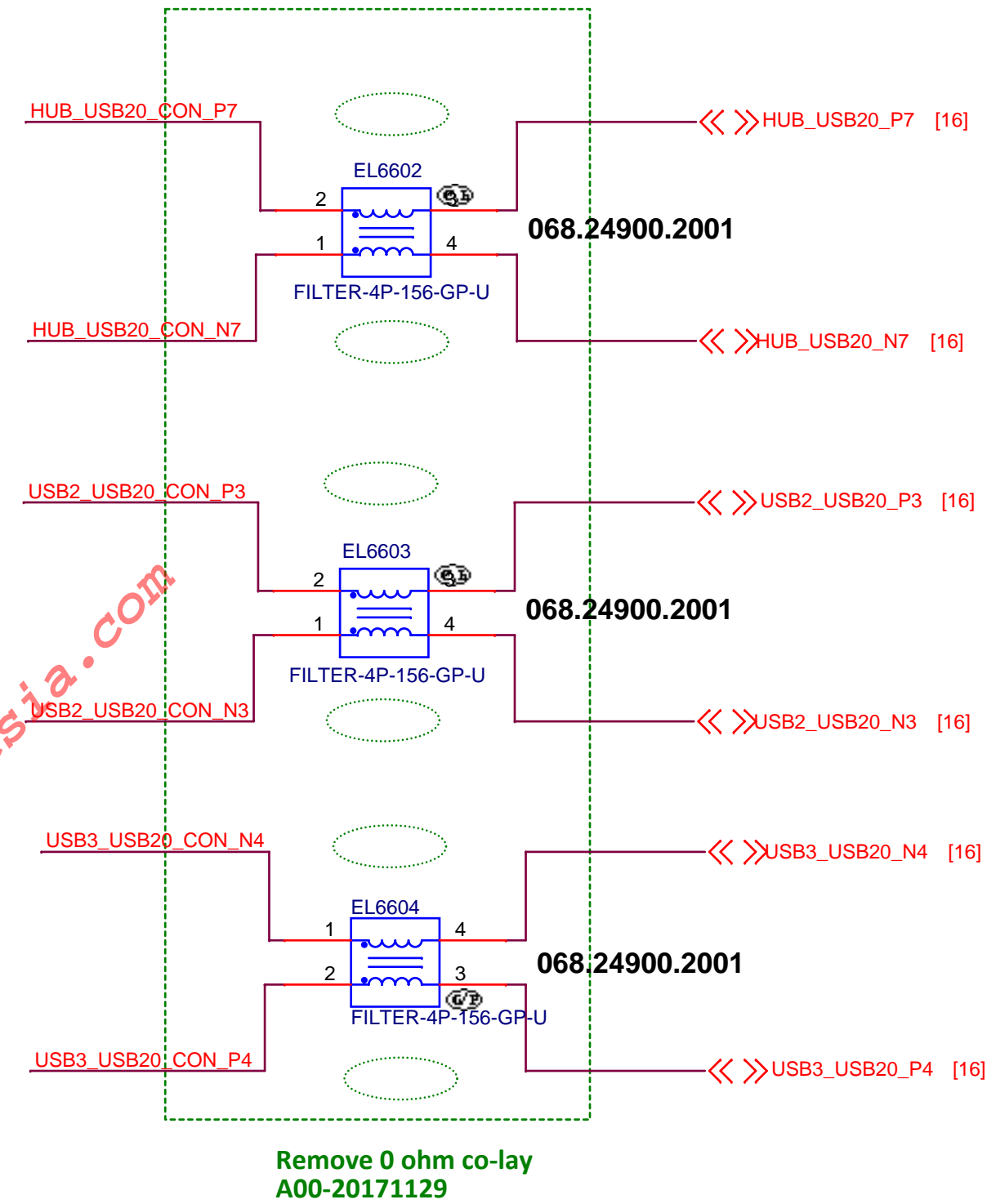
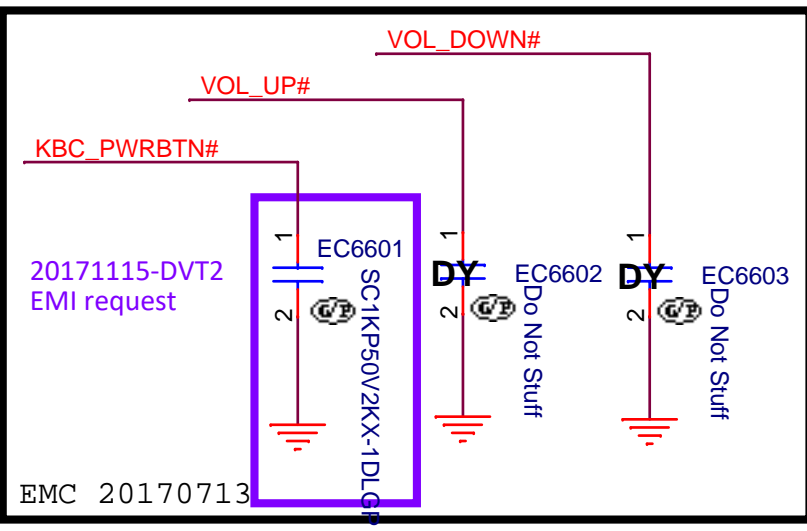
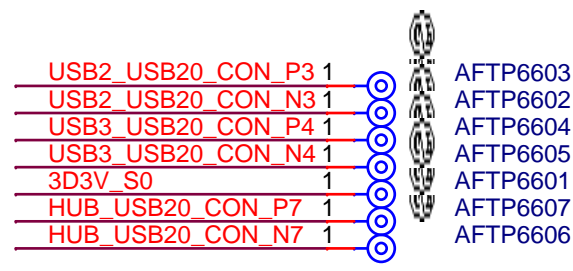
PIN#	SIGNAL
1	Diag_Loop=GPIO_1(TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [14] = KBD D15
23	KSO [9] = KBD D10
24	KSO [11] = KBD D12
25	KSO [10] = KBD D11
26	KSO [13] = KBD D14
27	CapsLock LED
28	N/C
29	N/C
30	GND





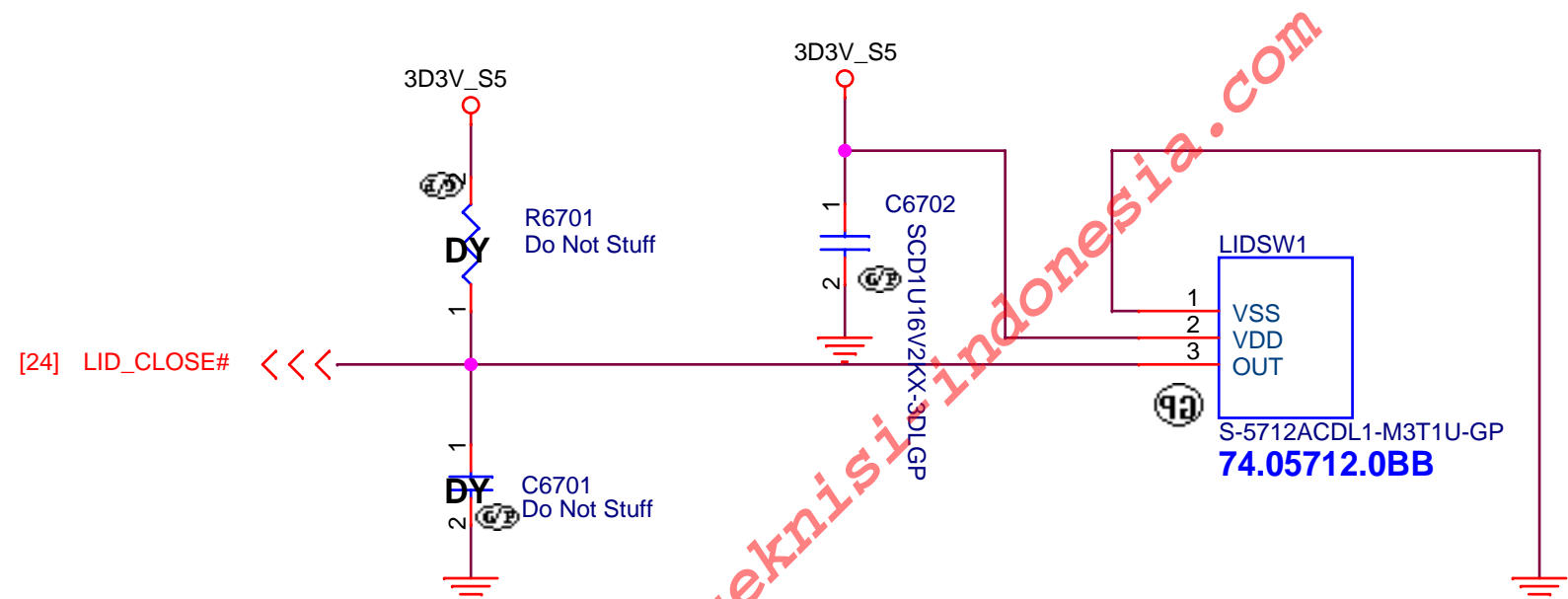


Power Pin Count : 8  
GND Pin Count : 8




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		Title <h2 style="text-align: center;">IO Board CONN</h2>	
Size A4	Document Number <b>Drax MLK/Rocket MLK AMD</b>		Rev <b>A00</b>
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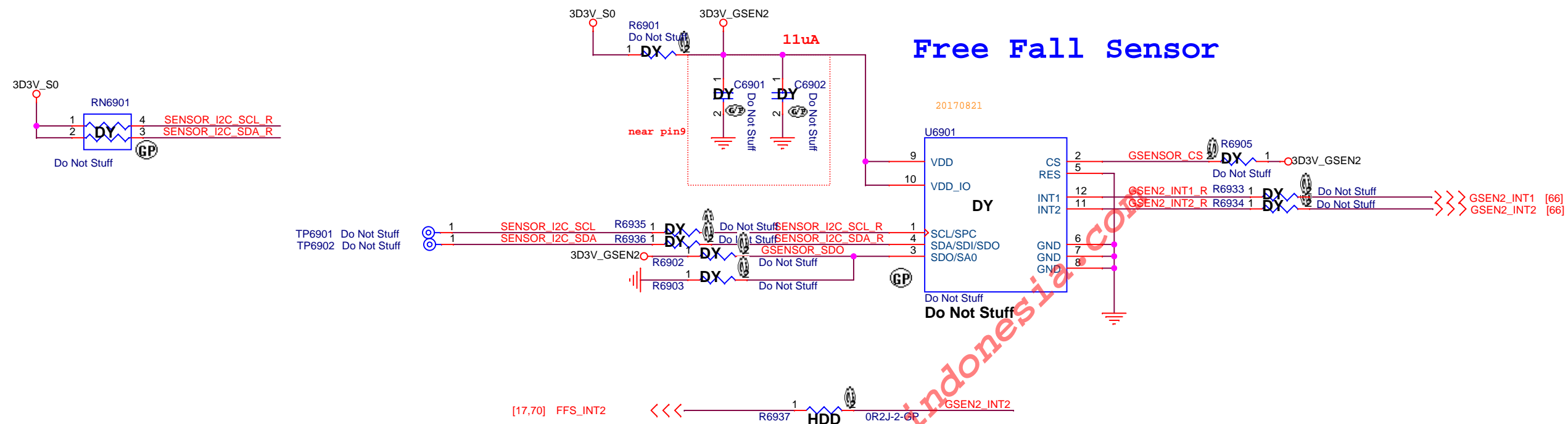
Drax Rocket MLK

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Title <b>Hall Sensor</b>			
Size A4	Document Number <b>Drax MLK/Rocket MLK AMD</b>		Rev <b>A00</b>
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**SSID = Sensor**



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<b>Title</b>	
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## FFS Sensor

Size  
A3

Document Number
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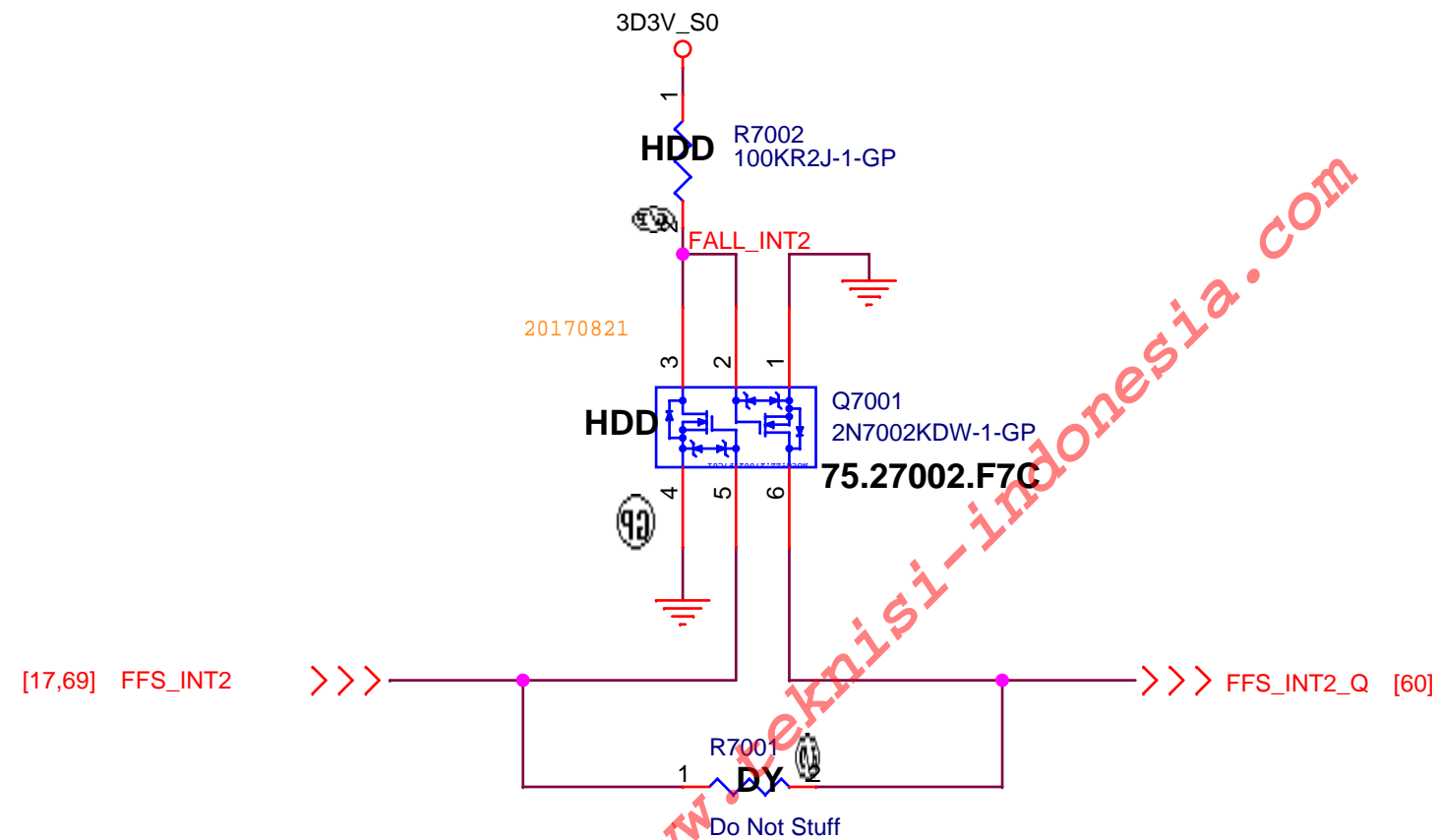
**Drax MLK/Rocket MLK AMD**

Rev  
**A00**

Date: Tuesday, January 02, 2018

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## SSID = Free Fall Sensor



## Drax Rocket MLK



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Taipei Hsien 221, Taiwan, R.O.C.

Title
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### ***Free Fall Sensor***

Size	A4
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Document Number

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Rev

400 |


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Title <b><i>(Reserved)Thunderbolt (1/5)</i></b>			
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Title <b>(Reserved)Thunderbolt (2/5)</b>			
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Title <b><i>(Reserved)Thunderbolt (3/5)</i></b>			
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Title <b><i>(Reserved)Thunderbolt (4/5)</i></b>			
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Title <b><i>(Reserved)Thunderbolt (5/5)</i></b>			
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Title <b>(Reserved)GPU (1/5) PEG</b>					
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Title			<b>(Reserved)GPU (2/5) DIGITAL</b>		
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Title <b><i>(Reserved)GPU (5/5) PWR/GND</i></b>			
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Title <b>(Reserved)VRAM1,2 (1/4)</b>			
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Title <b>(Reserved)VRAM3,4 (2/4)</b>			
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Title <b>(Reserved)VGA_CORE</b>					
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Title		<b>(Reserved)DISCRETE VGAPOWER</b>	
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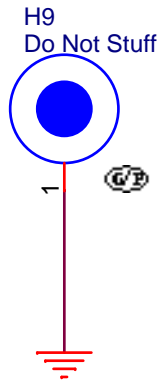
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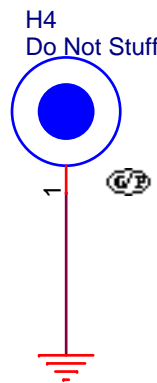
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Main Func = UnusedParts

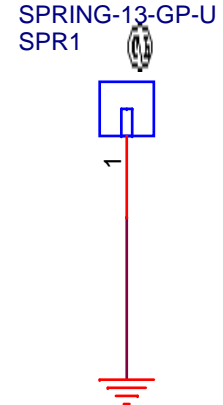
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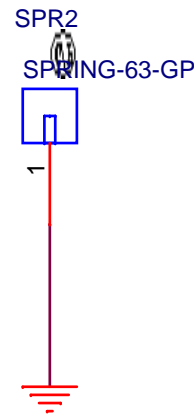


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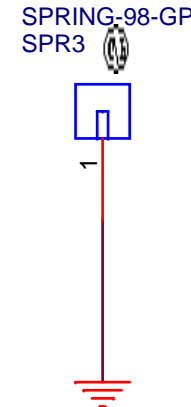


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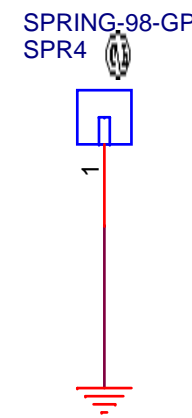
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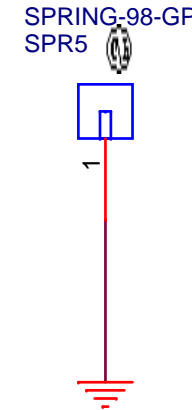
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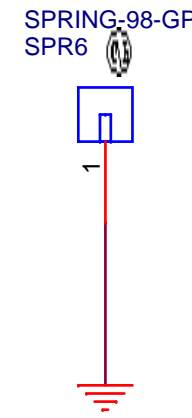
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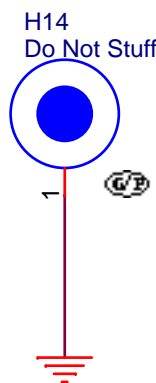
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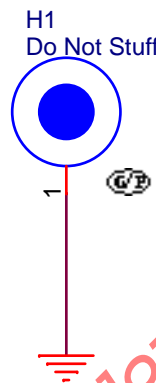
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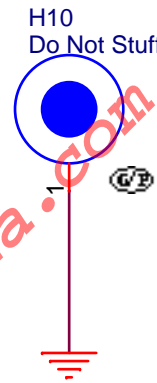
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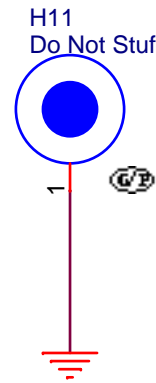
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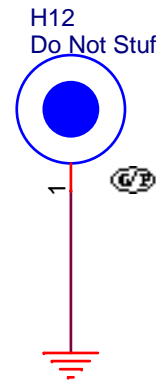
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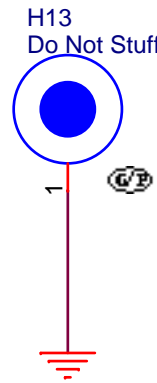
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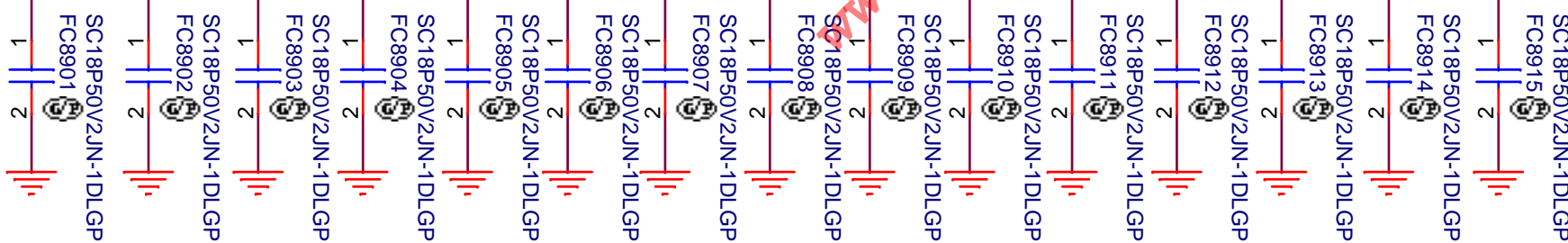
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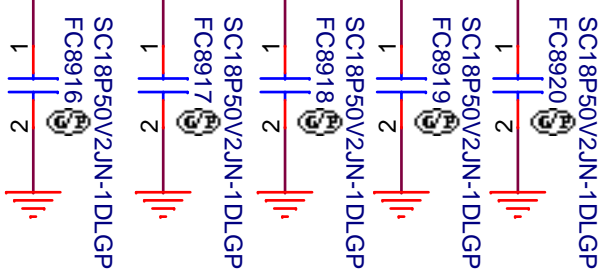
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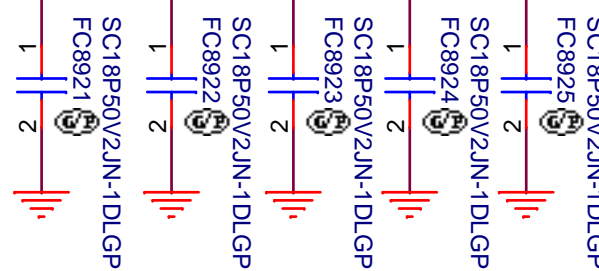
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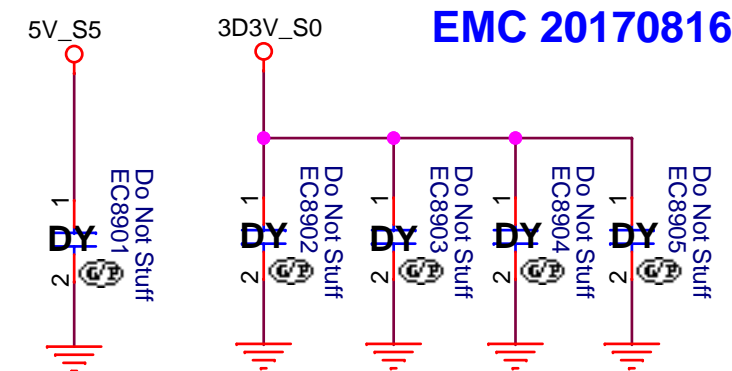
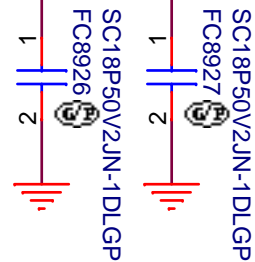
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Title <b>UNUSED PARTS/EMI Capacitors</b>		
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Title <b><i>(Reserved)NFC Connector</i></b>			
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Title <b>(Reserved) TPM</b>					
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Title

**(Reserved)Express Card**

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Title <b>(Reserved)Smart Card Socket</b>		
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Title <b>(Reserved)SW GFX eDP</b>			
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Title <b><i>(Reserved)Bottom Docking</i></b>			
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SSID = DEBUG PORT

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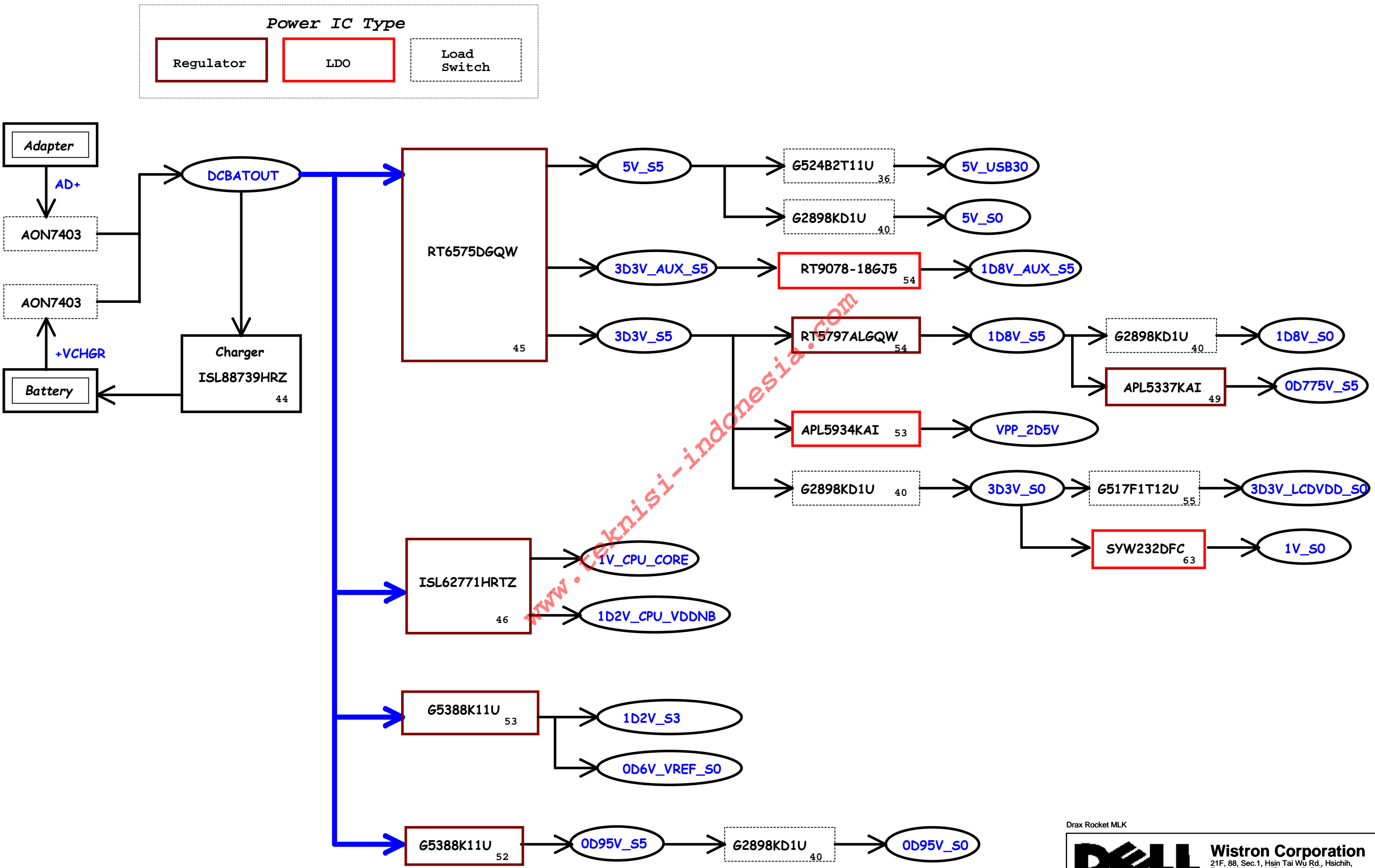
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Title <b>CPU XDP</b>		
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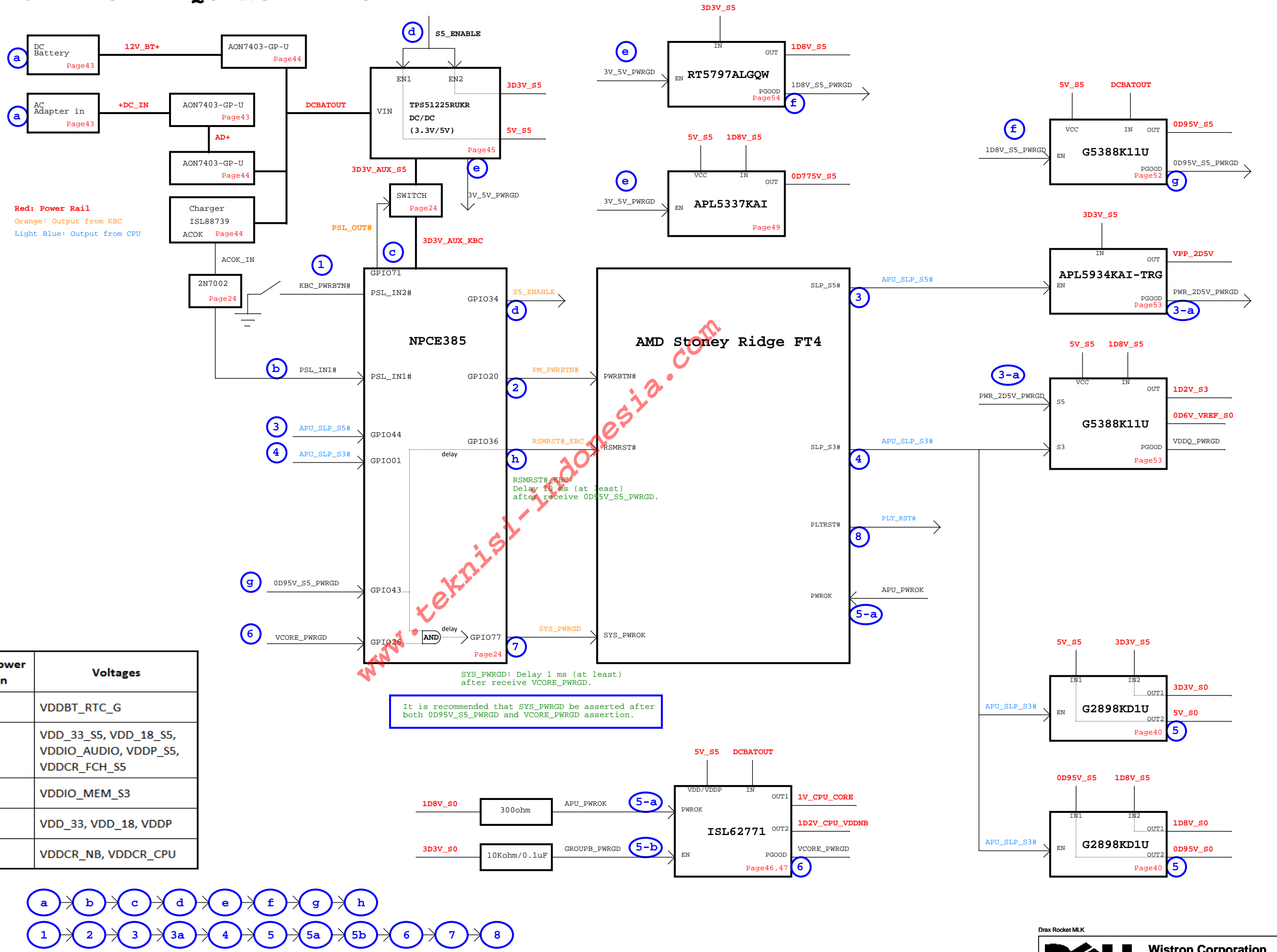
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004_(Reserved)	040_Power Plane Enable&Sequence	076_(Reserved)GPU(1/5) PEG
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006_(Reserved)	042_(Reserved)	078_(Reserved)GPU (3/5) VRAM I/F
007_CPU(VCC_CORE)	043_DCIN JACK & BATT Conn	079_(Reserved)GPU (4/5) GPIO/STRAP
008_CPU (DISPLAY/SVI2/JTAG/TES)	044_CHARGER ISL88739	080_(Reserved)GPU (5/5) PWR/GND
009_CPU (VSS)	045_TPS51225RUKR_5V/3D3V	081_(Reserved)VRAM1,2 (1/2)
010_CPU (Power CAP1)	046_ISL62771_CPUCORE(1/2)	082_(Reserved)VRAM3,4 (2/2)
011_(Reserved)	047_ISL62771_CPUCORE(2/2)	083_(Reserved)
012_DDR4-SODIMM1	048_(Reserved)	084_(Reserved)
013_(Reserved)DDR4-SODIMM2	049_VDDCRGFX_APL5337	085_(Reserved)GPU CORE_ISL62771HRTZ
014_(Reserved)	050_(Reserved)	086_(Reserved)DISCRETE VGAPOWER
015_(Reserved)	051_(Reserved)	087_(Reserved)
016_CPU(CLK/SATA/USB/SPI/LPC)	052_APW8861_0D95V	088_(Reserved)
017_CPU(ACPI/SD/AZ/GPIO/RTC)	053_VDDQ&VTT&VPP_APW8861	089_UNUSED PARTS/EMI Capacitors
018_(Reserved)	054_DC2DC_1D8V/1D5V	090_(Reserved)
019_(Reserved)	055_LCD/Inverter CONN	091_(Reserved)
020_CPU_Strappings	056_(Reserved)VGA	092_(Reserved)
021_(Reserved)	057_HDMI	093_(Reserved)
022_(Reserved)	058_(Reserved)	094_(Reserved)
023_(Reserved)	059_(Reserved)	095_(Reserved)
024_KBC_Nuvoton_NPCE385	060_SATA IF_HDD/ODD	096_(Reserved)
025_Flash(KBC+PCH)/RTC	061_NGFF_WLAN CONN	097_(Reserved)
026_THERMAL NCT7718W/Fan	062_(Reserved)	098_(Reserved)
027_Audio Codec ALC3204	063_(Reserved)	099_(Reserved)
028_(Reserved)	064_LED Board&Power Button	100_Table of Content
029_Speaker/HPMIC	065_Key Board&Touch Pad	101_Power Block Diagram
030_(Reserved)	066_IO Board Connector	102_Power Up Sequence Diagram
031_(Reserved)LAN RTL8111/RTL8106	067_(Reserved)	103_Power Down Sequence Diagram
032_(Reserved)RJ45&Transformer	068_Debug connector	104_SMBUS BLOCK DIAGRAM
033_Card Reader	069_(Reserved)	105_THERMAL/AUDIO BLOCK DIAGRAM
034_(Reserved) USB2.0 CONN	070_(Reserved)Hall Sensor	106_CLK / USB Block Diagram
035_USB3.0 CONN	071_(Reserved)	
036_USB Power SW	072_(Reserved)	

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Drax STR-FT4 POWER UP SEQUENCE DIAGRAM



Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_FCH_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_NB, VDDCR_CPU

It is recommended that SYS\_PWRGD be asserted after both 0D95V\_S5\_PWRGD and VCORE\_PWRGD assertion.



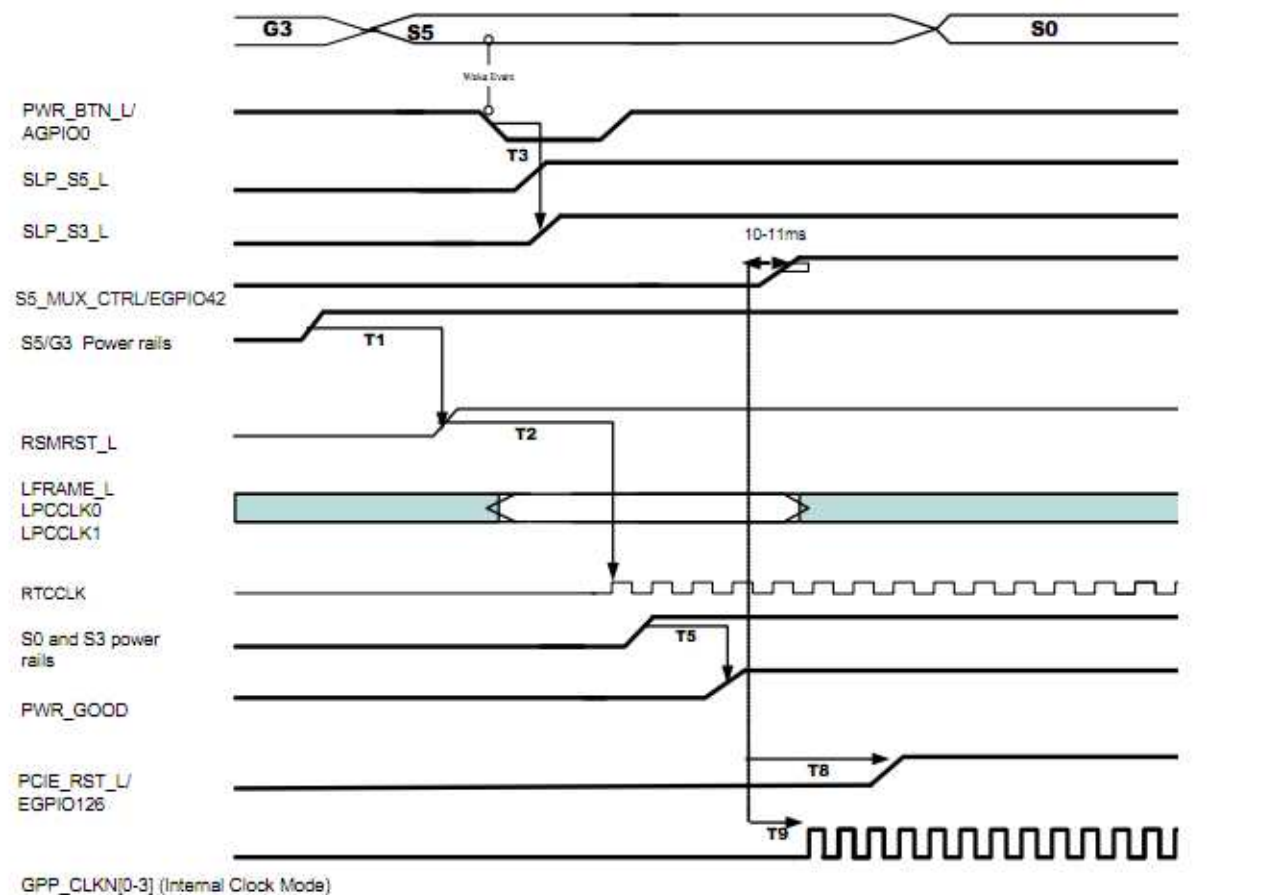


Table 58. G3->S5->S0 Reset Sequencing Timing Parameters without coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L. *This could take up to 5 seconds if power has been removed from VDDBT_RTC_G.
T2	16.5ms		15.5ms	From RSMRST_L to RTCCLK. *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126 (rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

Table 59. G3->S5->S0 Reset Sequencing Timing Parameter with coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L.
T2	16.5ms			From RSMRST_L to RTCCLK. *This timing is only valid if a Schmitt trigger is used or RC time constant of 10ms is used.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising).
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126(rising).
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

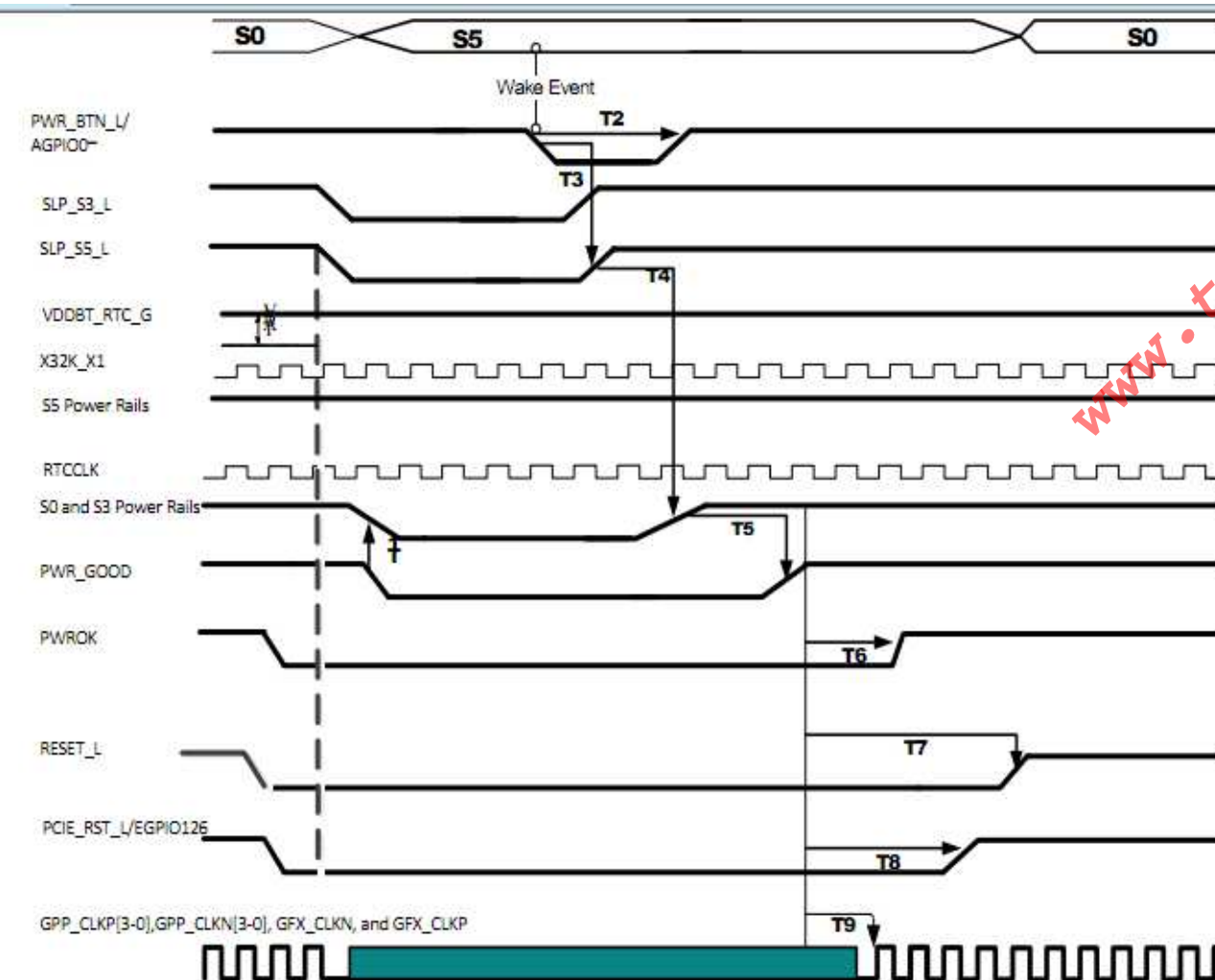


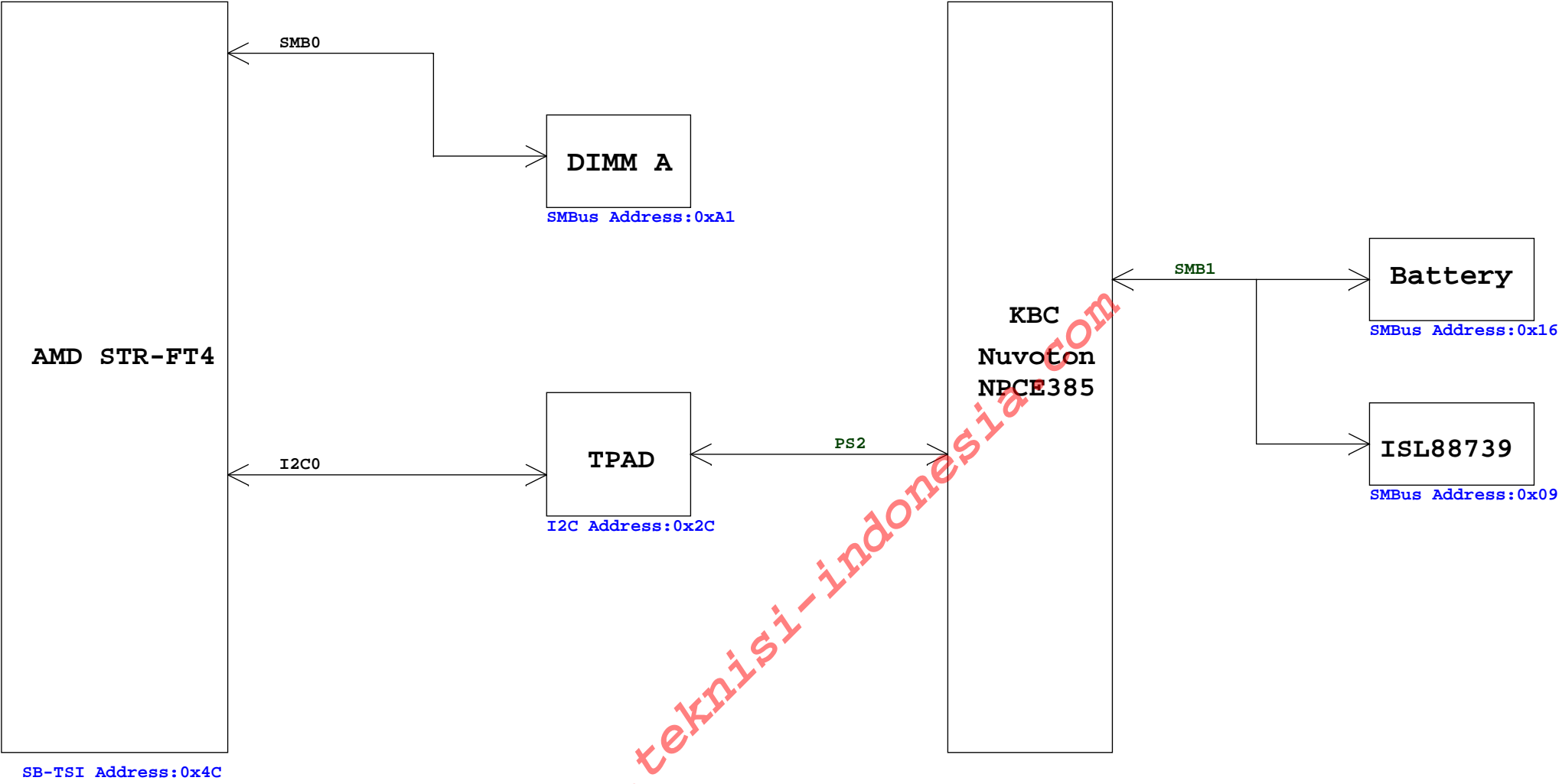
Figure 8. S0->S5->S0 Power Sequence Timing Diagram

Drax Rocket MLK

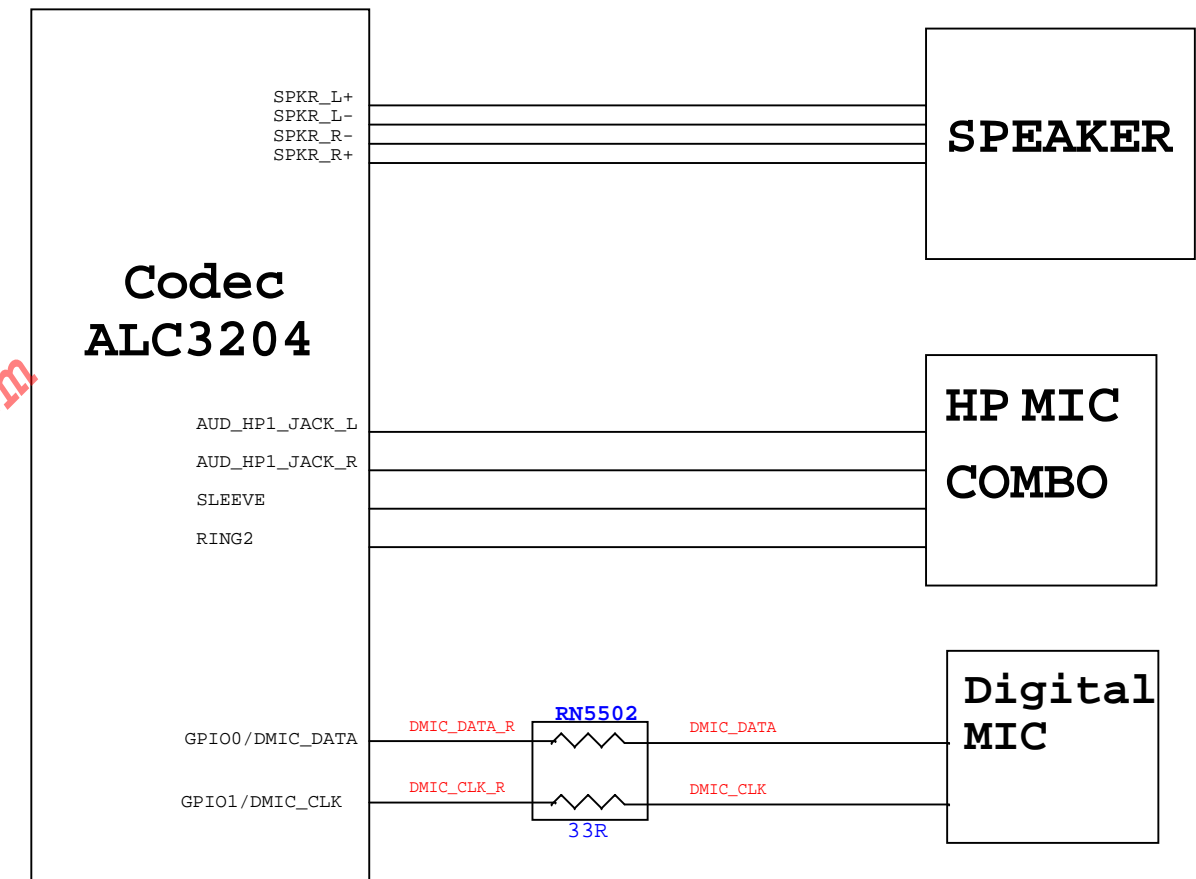


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Title			<b>Power Down Sequence</b>	
Size	Document Number		Rev	
	<b>Drax MLK/Rocket MLK AMD</b>		<b>A00</b>	
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## Audio Block Diagram



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Title			
<b>CLK / USB Block</b>			
Size	Document Number		Rev
A3	<b>Drax MLK/Rocket MLK AMD</b>		<b>A00</b>
Date:	Tuesday, January 02, 2018		Sheet 106 of 109

Date	Item	Change list and Desprition	Change Reasons
<b>X01</b>			
9/11/2017	1	PD4410 change to 75.00054.A7D	For common part
9/11/2017	2	PQ4415 change to 84.00024.A1K	For common part
9/11/2017	3	PQ4413 change to 84.T3906.E11	Power team request
9/11/2017	4	0402 0ohm change to 63.R0034.L0L ( 0 ohm,change to 13" tape-on-reel)	For factory need
9/20/2017	5	Add R2472(10Kohm) on PURE_HW_SHUTDOWN# signal	For PURE_HW_SHUTDOWN# signal
9/20/2017	6	R2492 change 20k to 47K	Solve 3D3V_AUX_S5 voltage drop
9/20/2017	7	Reserve C2448 (DY) on S5_ENABLE	Solve 3D3V_AUX_S5 voltage drop
9/20/2017	8	EC GPIO10 connect to LCD_TST	For panel BIST test
9/20/2017	9	EC GPIO50 connect to TOUCH_PANEL_EN	For panel BIST test
9/25/2017	10	PQ4301, Q5703 and Q5705 change to 084.00301.0031	For common part
9/25/2017	11	Delete SPR8, KB2, FAN1, SPK2, RTC2 connector and schematic	remove 13" colay components
9/25/2017	12	Q2604 (DY) and add R2476 & R2477 (0 ohm) for Thermal Sensor U2601's SMBUS	Solve CPU & thermal sensor SMBUS address conflicting problem
9/25/2017	13	Add TP2408, TP2409 for FAN_PWM1_C, FAN_TACH1_C	remove 13" colay components
9/25/2017	14	Add TP5501 for PROJECT_ID1 (For EC to check panel is 11" or 13")	remove 13" colay components
9/26/2017	15	PR4405 change to 64.16535.6DL	Power team fine tune Charger setting
9/26/2017	16	PR4603 change to 64.39005.6DL	Power team fine tune CPU PWR setting
9/26/2017	17	C1601, C1602 change to 78.15034.1FLDL (15pF) for CPU's 48MHz Crystal fine tune.	Crystal vendor fine tune result
9/26/2017	18	C1703, C1704, C6343, C6344 change to 78.18034.1FLDL(18pF) for CPU's 32.768KHz & SATA bridge IC's 30MHz Crystal fine tune.	Crystal vendor fine tune result
9/26/2017	19	R6365 change to 63.68134.1DL (680ohm) for SATA bridge IC's 30MHz Crystal fine tune.	Crystal vendor fine tune result
9/27/2017	20	Q2501 change to 75.00054.A7D	For common part
9/27/2017	21	Add R6110 for BLUETOOTH_EN signal, reserve R2478 and R6111 PU high 3.3V	Reserve Bluetooth control method.
9/28/2017	22	FC8901~FC8927 change BOM to 78.18034.1FLDL (18pF) for RF solution	RF solution
9/28/2017	23	R2499 (DY) , D2403 (DY) unused for fanless system (design for 13")	Mark components are deisgned for 13".
9/28/2017	24	Re-arrage IO board pin definition, add one pin RING2_R and one pin SLEEVE_R to improve audio performance test.	For Audio performance test result, vendor debug solution
10/2/2017	25	Reserve Q2506(084.02421.0031), Q2507(84.2N702.J31), R2516(63.10434.1DL), R2517(63.R0034.1DL), R2515 (0 ohm) for BIOS SPI ROM power supply optional solution.	Reserve BIOS SPI ROM's power opional solution for backup only.
10/2/2017	26	EC GPIO14 connect to INT_TP#_CONN	Solve TP wake up problem

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Title **Change History-01**

Size	Document Number	Rev
	<b>Drax MLK/Rocket MLK AMD</b>	<b>A00</b>
Date:	Tuesday, January 02, 2018	Sheet 107 of 109



5	4	3	2	1
Date	Item	Change list and Desprition	Change Reasons	
X02				
10/30/2017	1	R2437 Change to 33k	PCB version up to DVT2	
10/31/2017	2	0 ohm change to short pad ( 94 pcs ) for factory SMT request.	Factory SMT request	
11/3/2017	3	EC6506 Change to 100pf	EMC request, enhance ESD performance	
	4	SD_CD# add 1000pf (EC3301)	EMC request, enhance ESD performance	
11/3/2017	5	page12. 1D2V_S3 add 2pcs 18pf cap: FC1201, FC1202	RF request , enhance RF performance	
	6	page10. 3D3V_S5 add 2pcs 18pf cap: FC1001, FC1002	RF request , enhance RF performance	
	7	page10. 3D3V_S0 add 1pcs 18pf cap: FC1003	RF request , enhance RF performance	
	8	page24. 1D8V_AUX_S5 add 1pcs 18pf cap: FC2401	RF request , enhance RF performance	
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Title <b>Change History-02</b>				
Size	Document Number <b>Drax MLK/Rocket MLK AMD</b>			Rev <b>A00</b>
Date: Tuesday, January 02, 2018		Sheet 108 of 109		
5	4	3	2	1

Date	Item	Change list and Desprition	Change Reasons	Project	Category	Sub-Category	critical issues
A00							
11/29/2017	1	Page17. Remove TP1701	PSE had concern for test point location (too closed CPU). PSE agree to remove it.	Drax MLK_AMD		SMT concern	
	2	Page29. DY Q2901 C2902 R2905 Stuff R2914	improve audio jack detect time. (align schematic as Truis )	Drax MLK_AMD		Audio Jack detect	
	3	Page68. Change DB1 & HDT1 to solder mask dummy pad, and debug port circuit.	A00 do not need solder debug port.	Drax MLK_AMD		Debug port	
	4	Page24. Change R2437 to 100k	for A00 PCB VER AD	Drax MLK_AMD		PCB version	
	5	USB2.0 remove 0 ohm co-aly (remove R3501,R3502's PAD), USB3.0 remove CMC co-lay (remove EL3501's PAD . R3503,R3504 R change to shortPAD.)	A00 do not need co-lay	Drax MLK_AMD		USB EMI	
12/8/2017	6	Page16. DY FC1601	LPC CLK is for debug mode only. A00 will turn off debug mode( turn off CLK). RF test is OK.	Drax MLK_AMD		Debug port	
	7	Page60. add EC6002 22PF CAP	Reserve for EMI team	Drax MLK_AMD		EMI	
	8	Page61. R6112 R6113	WIFI/BT controlled by Driver, align with Starlord serise.	Drax MLK_AMD		WIFI/BT control	
	9	Page68. DY debug port & AMD HDT debug port circuit.	A00 DY debug solution	Drax MLK_AMD		Debug port	

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